Section 1 – Program Mission and Educational Objectives

Oregon Tech Mission:

Oregon Institute of Technology, an Oregon public university, offers innovative and rigorous applied degree programs in the areas of engineering, engineering technologies, health technologies, management, and the arts and sciences. To foster student and graduate success, the university provides an intimate, hands-on learning environment, focusing on application of theory to practice. Oregon Tech offers statewide educational opportunities for the emerging needs of Oregonians and provides information and technical expertise to state, national and international constituents.

Core Theme 1: Applied Degree Programs

Oregon Tech offers innovative and rigorous applied degree programs. The teaching and learning model at Oregon Tech prepares students to apply the knowledge gained in the classroom to the workplace.

Core Theme 2: Student and Graduate Success

Oregon Tech fosters student and graduate success by providing an intimate, hands-on learning environment, which focuses on application of theory to practice. The teaching and support services facilitate students' personal and academic development.

Core Theme 3: Statewide Educational Opportunities

Oregon Tech offers statewide educational opportunities for the emerging needs of Oregon's citizens. To accomplish this, Oregon Tech provides innovative and rigorous applied degree programs to students across the state of Oregon, including high-school programs, online degree programs, and partnership agreements with community colleges and universities.

Core Theme 4: Public Service

Oregon Tech will share information and technical expertise to state, national, and international constituents.

Program Mission: The mission of the Embedded Systems Engineering Technology (ESET) bachelor's degree program within the Computer Systems Engineering Technology (CSET) Department at Oregon Institute of Technology is to prepare our students for productive careers in industry and government by providing an excellent education incorporating industry-relevant, applied laboratory-based instruction in both the theory and application of embedded systems engineering. Our focus is educating students to meet the growing workforce demand in Oregon and elsewhere for graduates prepared in both hardware and software aspects of embedded systems. Major components of the ESET program's mission in the CSET Department are:

- To educate a new generation of ESET students to meet current and future industrial challenges and emerging embedded systems engineering trends.

- To promote a sense of scholarship, leadership, and professional service among our graduates.
- To enable our students to create, develop, apply, and disseminate knowledge within the embedded systems development environment.
- To expose our students to cross-disciplinary educational programs.
- To provide industry and government employers with graduates in embedded systems engineering and related professions.

Mission Alignment:

Our program is very hands-on and thus aligns with Core Theme 1. Our graduates are in high demand by the industries we support. This is evidence that we are aligned with Core Theme 2. The program features two years of project-based learning environment with junior project and senior project.

Section 2 – Program Description and History

Program History

The Embedded Systems Engineering Technology (ESET) program was proposed to OUS in spring of 2006 and approved in August, 2006. The curriculum for the ESET program is common with the hardware and software programs for the freshman year. The sophomore year of the ESET program has been constructed to mirror the track through both the Computer Engineering Technology (CET) and Software Engineering Technology (SET) programs, called the Concurrent Degree program. The ESET program junior year is when ESET students get instruction specific to topics of embedded systems engineering. These courses were taught for the first time in fall, 2008 on the Klamath Falls campus and soon after at the Wilsonville location. The full program is now offered to students at both locations.

Program Enrollment

Enrollment in the Embedded Systems Engineering Technology program has seen a 115.6% growth. Growth has been faster on the Portland-Metro campus versus the Klamath Falls, campus.

Oregon TECH

Computer Systems Eng Tech Headcount - Fall 4th Week
May 2, 2019

Student location is based on the primary campus assigned to each student; however students may enroll at other/multiple locations.
Majors with asterisk (*) have been phased out.
Dual Majors are reported under each separate major.

Computer Systems Eng Tech	Fall 2014	Fall 2015	Fall 2016	Fall 2017	Fall 2018
Computer Engineering Tech	**81**	**86**	**63**	**62**	**61**
Klamath Falls	77	78	57	60	57
Full-Time	68	70	51	50	48
Part-Time	9	8	6	10	9
Portland-Metro	4	8	6	2	4
Full-Time	1	8	4		
[illegible]	[illegible]		[illegible]	[illegible]	[illegible]
Embedded Systems Eng Tech	**32**	**35**	**57**	**57**	**69**
Klamath Falls	23	24	35	36	42
Full-Time	21	24	31	29	36
	2		4	7	6
Portland-Metro	9	11	22	21	27
Full-Time	2	4	11	10	14
Part-Time	7	7		11	13
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Klamath Falls	173	177	147	157	159
Full-Time	145	153	124	126	133
Part-Time	28	24	23	31	26
Portland-Metro	116	128	136	116	111
Full-Time	53	46	62	51	51
Part-Time	63	82	74	65	60
Grand Total	**402**	**426**	**403**	**392**	**400**

Figure 1 CSET Headcount

Program Graduates

Program graduates remained flat for both Embedded Systems and Computer Engineering Technology.

Oregon TECH

Computer Systems Eng Tech Degrees by Academic Year
May 6, 2019

Majors with asterisk (*) have been phased out.
Dual Majors are reported under each separate major.

Computer Systems Eng Tech	201314	201415	201516	201617	201718
Assoc of Engineering	**9**	**15**	**8**	**5**	**2**
Klamath Falls	8	12	7	4	2
Computer Engineering Tech	7	6	5	3	1
Software Engineering Tech	1	6	2	1	1
Portland-Metro	1	3	1	1	
Computer Engineering Tech			1		
Software Engineering Tech	1	3		1	
Bachelor of Science	**35**	**43**	**53**	**54**	**50**
Klamath Falls	22	29	30	26	21
Computer Engineering Tech	3	3	3	6	3
Embedded Systems Eng Tech	1	4	3	5	2
Software Engineering Tech	18	22	24	15	16
Portland-Metro	13	14	23	28	29
Embedded Systems Eng Tech		1		1	2
Software Engineering Tech	13	13	23	27	27
Grand Total	**44**	**58**	**61**	**59**	**52**

Figure 2 CSET Degrees

Employment Rates and Salaries

Institutional data indicates that graduates of the Embedded Systems Engineering Technology program are successful in finding employment. Some recent employers include Intel, Aristocrat, Mentor Graphics, LO3 Energy, Ravensclaw, Intel, Ravensclaw and Mentor Graphics. Some graduates are also pursuing graduate degrees in a related field.

Oregon Tech Graduate Outcome Data

a=2015 / 2016 / 2017 combined	% Employed		% Continuing Ed		% Seeking		% Not Seeking		Success Rate		Median Salary	
b=2016 / 2017 / 2018 combined	a	b	a	b	a	b	a	b	a	b	a	b
% among those reporting outcomes	**90.0**	**89.9**	**6.7**	**7.0**	**2.8**	**2.5**	**0.5**	**0.5**	**97.2**	**97.5**	**$ 58,000**	**$ 60,00**
Computer Engineering Technology	100	93	0	7	0	0	0	0	100		$ 64,000	$ 65,50
Embedded Systems Engineering Technology	88	75	13	13	0	13	0	0	100	87	$ 60,000	$ 60,00
Software Engineering Technology	93	89	0	1	5	8	2	2	95	92	$ 65,000	$ 67,00

Figure 3 Employment Data

Showcase Learning Experiences

- On April 4th, 2018 Larry Landis, Senior Manager at Intel PSG came to campus to give a talk on 'Getting hired in tech' as well as run a workshop on 'Timing Analysis'.
- On May 5th 2018, Junior project students participated in the campus wide project symposium to showcase their projects. Industry Advisory Board members were also invited to attend.

Program Changes

The program recently acquired the following new equipment towards the end of the 2018-2019 school year totaling $24,537.00 The equipment acquired will help keep labs up to date.

- 13 Rigol MSO1104 Mixed Signal Oscilloscopes
- 11 Rigol DG1022Z 25 MHz Waveform Generators
- 13 Rigol DP832 Programmable DC Power Supplies
- 2 Pico 2205A Picoscopes
- 20 ICD4 Programmer/Debugger
- 20 Explorer 16/32 Development boards with PIC32MX460 processors
- 2 Chipwhisperer Lites
- 10 UNI-T UT61E Multimeters
- 2 Salae Logic Analyzer

Intel PSG also recently donated 10 DE10-Lites and 2 Stratix 10 development boards. The DE10-Lite boards will be used for CST 162/133 Digital Logic I/II. The Stratix 10 will be used in CST 351.

George Drouant was hired as Instructor on the Klamath Falls campus. He will teach CST 130, CST 131, CST 204, CST 250, CST 315, and other courses to support the Computer Engineering Technology and Embedded Systems Engineering Technology programs. Below is his background.

EDUCATION

- M.S. Engineering and Applied Sciences, University of New Orleans
- M.S. Biomedical Engineering, Tulane University
- M. E. Electrical Engineering, Tulane University
- B.S. Engineering Science, University of New Orleans
- Pursuing Ph.D. in Engineering and Applied Sciences, University of New Orleans
- Research Area: Signal processing of Sperm Whale echolocation clicks

BACKGROUND

- Over 25 years industry experience at companies which include Lockheed Martin, Jacobs Engineering, LSU Health Science Center, and Tulane Medical School
- Licensed Professional Engineer in Electrical Engineering

Program Improvement Discussions

On September 18, 2019 Enrollment was discussed. ESET enrollment was up 115.6% and CET enrollment was down 24.6%.

CET faculty discussed why enrollment was down. Ideas mentioned were 'Embedded is the hot topic right now'. It was suggested that we investigate what other schools are doing, and further investigate how we can move enrollment in a positive direction. However, the main concern we expressed was that the Technology is the biggest impediment to program success for the Computer Engineering Technology program.

Program faculty discussed CST 136 and EE 321. It was decided that students may end up in different roles and perhaps through advising students could choose to take CST 136 or EE 321. This change is approved pending discussions with EERE.

We discussed offering microcontrollers for EERE but also noted the challenge of our pre-requisite chain.

Industry Advisory Board Meeting

On May 5, 2018 at 9 AM, we held our department IAB meeting to discuss key issues affecting our programs.

Key issues discussed included:

1. Management proposed a reduction of CST 337 and CST 331 from 5 credits to 4 credits, eliminating one lab section. IAB strongly voiced their opinion in opposition of this change. They indicated the hands-on time with Doug Lynn was one of the crucial pieces of developing their engineering skills.
2. Wire wrapping is not really necessary as modern designs are spun out to PCB.
3. We discussed a shift to the Engineering degree which has been awaiting approval. IAB voiced their opinion in support of moving towards Engineering.
4. IAB indicated that removal of CST 136 was a bad idea if it was not replaced with something of similar value.

IAB notes were reviewed on September 18, 2019 by program faculty. One proposed item in question was regarding reducing the CST 337 and CST 331 labs from two labs per week to one lab per week. CET and ESET faculty determined that reducing lab time would result in a negative impact to the program learning outcomes and that it should not be implemented. Doug Lynn, the instructor of both classes indicated that the labs would need to be reduced in intensity and would need to become turnkey, resulting in reduced learning.

Core Program Faculty

Douglas Lynn, Professor (KF)

Michael Healy, Assistant Professor (KF)

Phong Nguyen, Assistant Professor (PM)

Kevin Pintong, Program Director Computer Engineering Technology, Associate Professor (KF)

George Drouant, Instructor (KF)

Pramod Govindan, Instructor (PM)

Troy Scevers, Program Director Embedded Systems Engineering Technology, Associate Professor (KF)

Section 3 – Program Student Learning Outcomes

The mission of the Embedded Systems Engineering Technology (ESET) Degree program within the Computer Systems Engineering Technology (CSET) Department at Oregon Institute of Technology is to prepare our students for productive careers in industry and government by providing an excellent education incorporating industry-relevant, applied laboratory based instruction in both the theory and application of embedded systems engineering. Our focus is educating students to meet the growing workforce demand in Oregon and elsewhere for graduates prepared in both hardware and software aspects of embedded systems. Major components of the ESET program's mission in the CSET Department are:

1. To educate a new generation of Embedded Systems Engineering Technology students to meet current and future industrial challenges and emerging embedded systems engineering trends.
2. To promote a sense of scholarship, leadership, and professional service among our graduates.
3. To enable our students to create, develop, apply, and disseminate knowledge within the embedded systems development environment.
4. To expose our students to cross-disciplinary educational programs.
5. To provide government and high tech industry employers with graduates in embedded systems engineering and related professions.

Program Educational Objectives

The Program Educational Objectives reflect those attributes a student of the ESET program will practice in professional endeavors.

- Graduates of the ESET program are expected to understand the societal impact of embedded systems and technological solutions.
- Graduates of the ESET program are expected to do hardware/software co-design for embedded systems. Graduates will continue to develop skills in analysis, approach, optimization, and implementation of embedded systems.
- Graduates of the ESET program are expected to obtain the knowledge, skills and capabilities necessary for immediate employment in embedded systems
- Graduates of the ESET program are expected to participate in life-long learning to be able to adapt to a changing environment.

Program Student Learning Outcomes

(1) an ability to apply knowledge, techniques, skills and modern tools of mathematics, science, engineering, and technology to solve well-defined engineering problems appropriate to the discipline; (ESLO Inquiry and Analysis)

(2) an ability to design solutions for well-defined technical problems and assist with the engineering design of systems, components, or processes appropriate to the discipline;

(3) an ability to apply written, oral, and graphical communication in well-defined technical and non-technical environments; and an ability to identify and use technical literature; (ESLO Communication)

(4) an ability to conduct standard tests, measurements, and experiments and to analyze and interpret the results; (ESLO Quantitative Literacy)

(5) an ability to function effectively as a member of a technical team. (ESLO Teamwork)

Program Student Learning Outcomes Update

On September 18, 2019, the ESET and CET faculty met to review and approve changes to the mission statement, and program student learning outcomes. The ABET ETAC a-k were updated to reflect changes to ABET ETAC 1-5 as of the 2019-2020 cycle. These changes will be discussed in the Fall 2019 Industry Advisory Board.

External validation

External validation of PSLO are achieved through the following:

1) Industry Advisory Board discussions
2) Graduate job placement and continuing education rates
3) PSLO are aligned and updated to reflect changes to ABET ETAC 2019-2020 Cycle.

Section 4 – Curriculum Map

Program Student Learning Outcomes

Course	Major	Title	PSLO				
			1	2	3	4	5
CST 162		Digital Logic I	X				
CST 130		Computer Organisation	X				
CST 120		Embedded C	X				
CST 131		Computer Architecture	X				
CST 133		Digital Logic II	X	x			
CST 134		Instrumentation	X			X	
CST 250		Computer Assembly Language	X	x			
CST 204		Introduction to Microcontrollers	X	x	x		
CST 231		Digital Systems Design I	X		X		
CST 337		Embedded System Architecture	X	X	x	X	
CST 315		Embedded Sensor Interfacing & I/O	X			X	
CST 374		Embedded Project Proposal	X		X		
CST 371		Embedded Systems Development 1 (Junior Project)	X		X	X	X
CST 372		Embedded Systems Development 2 (Junior Project)	X		X		X
CST 373		Embedded Systems Development 3 (Junior Project)	X		X		X
CST 471		Embedded Senior Project 1	X		X		
CST 472		Embedded Senior Project 2	X		X		
CST 473		Embedded Senior Project 3	X		X		
CST 331	CpE	Microprocessor Peripheral Interfacing	X	X	x	X	
CST 418	CpE	Data Comm & Networks	X				
CST 351	CpE	Digital System Design II	X		x		
CST 344	CpE	Intermediate Computer Architecture	X				
CST 442	CpE	Advanced Computer Architecture	X				
CST 455	ES	System on a Chip Design	X				
CST 456	ES	Embedded System Testing	X				
CST 466	ES	Embedded System Security	X		X	x	
CST 417	ES	Embedded Networking	X				
CST 347	ES	Real Time Embedded Operating Systems	X				

X = Major component, x = minor component

The curriculum map was updated and approved on October 4, 2019.

Essential Student Learning Outcomes

Essential student learning outcomes are given in the table below at the introduction, practice, and capstone levels.

ESLO	Introduction	Practice	Capstone
Communication	WRI 121, WRI 122, SPE 111	WRI 227 CST 371/372/373/374	WRI 327 (CET) / WRI 350 (ESET) CST 471/472/473
Inquiry and Analysis	All CST 1xx	All CST 2xx	All CST 3xx/4xx
Ethical Reasoning	CST 371	PHIL 331 - CET CST 372/373	CST 471/472/473
Teamwork	SPE 321	CST 371, CST 372	CST 373
Quantitative Literacy	MATH 111/112	MATH 251/252/253	Adv. Math Elective or MATH 465
Diverse Perspectives	ANTH 452/ BUS 304	CST 371/372/373	CST 471/472/473

Section 5 – Assessment Cycle

The table below is the updated assessment cycle for 2019-2022. The assessment cycle below reflects changes made as a result of the ABET ETAC a-k to 1-5 learning outcomes change. PSLO are assessed in a three year cycle and the ESLO are assessed in a six year cycle. Each PSLO will have two direct measurements (two classes) with one indirect measurement, and each ESLO will have one direct measurement.

PSLO	ESLO	2019-2020	2020-2021	2021-2022
(1) an ability to apply knowledge, techniques, skills and modern tools of mathematics, science, engineering, and technology to solve well-defined engineering problems appropriate to the discipline; (ESLO Inquiry and Analysis)	**Inquiry and Analysis**			**CET/ESET: CST 133 (Kevin, Pramod)** **CET: CST 334, 442, 418 (Doug)** **ESET: CST 456**
(2) an ability to design solutions for well-defined technical problems and assist with the engineering design of systems, components, or processes appropriate to the discipline;		**CST 315 (Pramod, George)** **CST 473 (Kevin, Phong)**		**CST 315 (Pramod, George)** **CST 473 (Kevin, Phong)**
(3) an ability to apply written, oral, and graphical communication in well-defined technical and non-technical environments; and an ability to identify and use appropriate technical literature; (ESLO Communication)	**Communication**	**CST 371 (Mike, Phong)** **CST 473 (Kevin, Phong)**		
(4) an ability to conduct standard tests, measurements, and experiments and to analyze and interpret the results; (ESLO Quantitative Literacy)	**Quantitative Literacy**		**ESLO** **CST 337 (Doug)** **CST 134 (George, Pramod)**	
(5) an ability to function effectively as a member of a technical team. (ESLO Teamwork)	**Teamwork**	**ESLO** **CST 371 (Mike, Phong)**	**CST 371 (Mike, Phong)** **CST 231 (Kevin, Pramod)**	
N/A	**Diverse Perspectives**			**CST 471 (Kevin, Phong)**
N/A	**Ethical Reasoning**	**-**	**-**	**-**

Section 6 – Assessment Activity

This year's assessment focused on the learning outcomes below. Note that this follows the a-k ABET from 2018-2019 assessment cycle. We will be assess using the 2019-2020 PSLOs in 2019-2020.

Reference the following table and page numbers. Indirect assessment is provided as Student Exit survey in appendix. The indirect assessment for A,D,E,K indicate that we are meeting the PSLO, although due to small sample size it is not statistically strong.

Assessment	**Program Student Learning Outcomes** **3-year cycle** **Computer/Embedded Systems Engineering Technology B.S.**	**2018-19**	**Page**	**Status**
A	An ability to select and apply the knowledge, techniques, skills, and modern tools of the discipline to broadly-defined engineering technology activities;	471 (Kevin, Phong) 371 (Mike, Phong)	**6, 7** **8,9**	**OK** **OK**
D	An ability to design systems, components, or processes for broadly-defined engineering technology problems appropriate to program educational objectives;	471 (Kevin, Phong) 371 (Mike, Phong)	**10,11** **12,13**	**OK** **OK**
E	An ability to function effectively as a member or leader on a technical team;	372 (Phong, Mike) 373 (Phong, Mike)	**14,15**	**OK** **OK**
K	A commitment to quality, timeliness, and continuous improvement.	473 (Kevin, Phong) 373 (Phong, Mike)	**16, 17** **18, 19**	**Investigate KF** **OK**

Assessment A – KF - 471

Learning Outcome: An ability to select and apply the knowledge, techniques, skills, and modern tools of the discipline to broadly-defined engineering technology activities

Course/Event: CST 471-473

Level: Capstone

Assessor & Campus: Kevin Pintong at Klamath Falls

Activity: Student submitted final project status memo (requirements) and final project report(Control/innovation) for year-long project.

Rubric:

1. Project Final Status Memo- Determine how many requirements out of original proposed were met. Score = # requirements met / # requirements not met.
2. Timely completion- Did the student successfully complete and demonstrate the project at end of term? Yes = 100% No = 0%
3. Final project report grade – See Appendix B.

Sample and Reliability: Ten student artifacts assessed. Limited sample size may skew results. Scoring was performed by faculty of record for CST 471.

Multiple Sites: Terminology used in assignments are different but same content was covered.

Performance Target: Student achieve grade of > 75% according to rubrics for each item.

Performance Level:

Item		ESET	CET
1	Project Final Status Memo	100% (3/3)	83% (5/6)
2	Timely completion	100% (3/3)	83% (5/6)
3	Final Project Report	67% (2/3)	67% (4/6)
	Overall	88%	77%

History of Results: Not Available.

Faculty Discussion: Results are discussed in next cycle.

Interpretation: Data provided in this report indicates that the Program Student Learning Objectives are being met for Klamath Falls. Limited sample size.

Assessment A – WL - 471

Learning Outcome: An ability to select and apply the knowledge, techniques, skills, and modern tools of the discipline to broadly-defined engineering technology activities

Course/Event: CST 471-473

Level: Capstone

Assessor & Campus: Phong Ngyuen at Wilsonville

Activity: Student submitted Plan, Schedule and Control documents for team-choice, year-long Embedded Project requiring Input, Output, Processor, Control to innovate and/or improve technology.

Rubric: See Appendix A.

Sample and Reliability: 4 student artifacts assessed. Limited sample size may skew results. Scoring was performed by faculty of record for CST 471.

Multiple Sites: Terminology used in assignments are different but same content was covered.

Performance Target: Student achieve grade of > 80% according to rubrics

Performance Level:

Item		ESET	CET
1	Plan	80%	NA
2	Schedule	80%	NA
3	Control	85%	NA
	Overall	4 of 4	NA

History of Results: Not Available.

Faculty Discussion: Results are discussed in next cycle.

Interpretation: Data provided in this report indicates that the Program Student Learning Objectives are being met for Wilsonville. There were time delays in one project. Need to speed up.

Assessment A – KF - 371 – Direct

Learning Outcome: An ability to select and apply the knowledge, techniques, skills, and modern tools of the discipline to broadly-defined engineering technology activities

Course/Event: CST 371

Level: Capstone

Assessor & Campus: Mike Healy at Klamath Falls

Activity: Student submitted Plan, Schedule and Control documents for team-choice, year-long Embedded Project requiring Input, Output, Processor, Control to innovate and/or improve technology.

Rubric: See Appendix C.

Sample and Reliability: Four student artifacts assessed. Limited sample size may skew results. Scoring was performed by faculty of record for CST 371.

Multiple Sites: Terminology used in assignments are different but same content was covered.

Performance Target: Achieve grade of > 80% according to rubrics

Performance Level:

CST 371

Item		ESET	CET
1	Plan	96%	95%
2	Schedule	100%	100%
3	Control	95%	95%
		4 of 4	--

Successful performance criteria: 85% of teams were able to achieve >80/100 in documents

Students were rated on a point scale on rubric for each document

History of Results: Not Available.

Faculty Discussion: Results are discussed in next cycle.

Interpretation: Data provided in this report indicates that the Program Student Learning Objectives are being met for Klamath Falls.

Assessment A- WL - 371 - Direct

Learning Outcome: An ability to select and apply the knowledge, techniques, skills, and modern tools of the discipline to broadly-defined engineering technology activities

Course/Event: CST 371

Level: Capstone

Assessor & Campus: Phong Ngyuen at Wilsonville

Activity: Student submitted Plan, Schedule and Control documents for team-choice, year-long Embedded Project requiring Input, Output, Processor, Control to innovate and/or improve technology.

Rubric: See Appendix A.

Sample and Reliability: 4 student artifacts assessed. Limited sample size may skew results. Scoring was performed by faculty of record for CST 371.

Multiple Sites: Terminology used in assignments are different but same content was covered.

Performance Target: Achieve grade of > 80% according to rubrics

Performance Level:

CST 371

Item		ESET	CET
1	Plan	90%	NA
2	Schedule	85%	NA
3	Control	85%	78%
		3 of 3	NA

Successful performance criteria: 85% of teams were able to achieve >80/100 in documents

Students were rated on a point scale on rubric for each document

History of Results: Not Available.

Faculty Discussion: Results are discussed in next cycle.

Interpretation: Data provided in this report indicates that the Program Student Learning Objectives are being met for Wilsonville.

Assessment D – KF – 471 - Direct

Learning Outcome: An ability to design systems, components, or processes for broadly-defined engineering technology problems appropriate to program educational objectives;

Course/Event: CST 471-473

Level: Capstone

Assessor & Campus: Kevin Pintong at Klamath Falls

Activity: Final Status Project Memo

Rubric: Is the project functional? Functionality was determined by calculating percentage of original requirements completed. See Appendix B

Sample and Reliability: Nine student artifacts assessed. Limited sample size may skew results. Scoring was performed by faculty of record for CST 471.

Multiple Sites: Terminology used in assignments are different but same content was covered.

Performance Target: Achieve grade of > 75% original requirements completed.

Performance Level:

Item		ESET	CET
1	Project Final Status Memo (% requirements complete)	100% (3/3)	67% (4/6)

History of Results: Not Available.

Faculty Discussion: Results are discussed in next cycle.

Interpretation: Data provided in this report indicates that the Program Student Learning Objectives are being met for Klamath Falls. One student was not able to complete the project on time and was given an incomplete. Another student achieved a grade of 65% of original requirements completed, which was the minimum standard set to pass the class.

Given the limited sample size, there is insufficient information to determine whether a change needs to be made to the assessment or the way by which the course is taught.

Assessment D – WL - 471

Learning Outcome: An ability to design systems, components, or processes for broadly-defined engineering technology problems appropriate to program educational objectives;

Course/Event: CST 471-473

Level: Capstone

Assessor & Campus: Phong Ngyuen at Wilsonville

Activity: Senior and Junior projects were required to complete devices built to satisfy all specifications of proposal. Also, projects were completed by using guidelines established by plan, schedule and control documents. All projects are intellectual property of students. If requested, students will demonstrate projects. As an example, below are photos of project, poster and members of one Junior Project team. Project was a Retrograde Game Console.

Rubric: Is the project functional?

Sample and Reliability: Ten student artifacts assessed. Limited sample size may skew results. Scoring was performed by faculty of record for CST 471.

Multiple Sites: Terminology used in assignments are different but same content was covered.

Performance Target: Achieve grade of > 75% according to rubrics for each item.

Performance Level:

Item		ESET	CET
1	Project successfully demoed and functional.	100% (4/4)	N/A
	Overall	100% (4/4)	N/A

History of Results: Not Available.

Faculty Discussion: Results are discussed in next cycle.

Interpretation: Data provided in this report indicates that the Program Student Learning Objectives are being met for Wilsonville. There were time delays in one project. Need to speed up.

Assessment D – KF - 371

Learning Outcome: An ability to select and apply the knowledge, techniques, skills, and modern tools of the discipline to broadly-defined engineering technology activities

Course/Event: CST 371-373

Level: Capstone

Assessor & Campus: Mike Healy at Klamath Falls

Activity: Student submitted Plan, Schedule and Control documents for team-choice, year-long Embedded Project requiring Input, Output, Processor, Control to innovate and/or improve technology.

Rubric: See Appendix C

Sample and Reliability: Four student artifacts assessed. Limited sample size may skew results. Scoring was performed by faculty of record for CST 371.

Multiple Sites: Terminology used in assignments are different but same content was covered.

Performance Target: Achieve grade of > 80% according to rubrics

Performance Level:

Item		ESET	CET
1	Plan	96%	95%
2	Schedule	100%	100%
3	Control	95%	95%
	Overall	4 of 4	--

History of Results: Not Available.

Faculty Discussion: Results are discussed in next cycle.

Interpretation: Data provided in this report indicates that the Program Student Learning Objectives are being met for Klamath Falls.

Assessment D – WL - 371

Learning Outcome: An ability to select and apply the knowledge, techniques, skills, and modern tools of the discipline to broadly-defined engineering technology activities

Course/Event: CST 471-473

Level: Capstone

Assessor & Campus: Phong Ngyuen at Wilsonville

Activity: Student teams submitted Plan, Schedule and Control documents for team-choice, year-long Embedded Project requiring Input, Output, Processor, Control to innovate and/or improve technology.

Rubric: See Appendix A.

Sample and Reliability: 3 student artifacts assessed. Limited sample size may skew results. Scoring was performed by faculty of record for CST 371.

Multiple Sites: Terminology used in assignments are different but same content was covered.

Performance Target: Achieve grade of > 80% according to rubrics

Performance Level:

Item		ESET	CET
1	Plan	90%	NA
2	Schedule	85%	NA
3	Control	85%	NA
		3 of 3	NA

History of Results: Not Available.

Faculty Discussion: Results are discussed in next cycle.

Interpretation: Data provided in this report indicates that the Program Student Learning Objectives are being met for Wilsonville.

Assessment E – KF - 372 and 373 – Direct

Learning Outcome: An ability to function effectively as a member or leader on a technical team;

Course/Event: CST 372 and 373

Level: Capstone

Assessor & Campus: Mike Healy at Klamath Falls

Activity: Peer Evaluation.

Rubric: Student evaluation surveys were conducted by team members on other team members. Also papers on lessons learned, lay-language project descriptions, and testing were assigned. See appendix for sample submission of a Student Evaluation. Other papers can be provided on request. See Appendix G.

Sample and Reliability: Fourteen student artifacts assessed. Limited sample size may skew results. Scoring was performed by faculty of record for CST 372/373.

Multiple Sites: Terminology used in assignments are different but same content was covered.

Performance Target: Achieve grade of > 75% original requirements completed.

Performance Level:

Item		ESET	CET
1	Peer Evaluations (% requirements complete)	100% (10/14)	100% (4/14)

History of Results: Not Available.

Faculty Discussion: All team members of all three groups graded all other team members > 75%. Also, papers were overwhelmingly positive.

Interpretation: Data provided in this report indicates that the Program Student Learning Objectives are being met for Klamath Falls. Professor evaluations of each team member was also completed.

Assessment E – WL - 372 and 373 - Direct

Learning Outcome: An ability to function effectively as a member or leader on a technical team;

Course/Event: CST 372 and 373

Level: Capstone

Assessor & Campus: Phong Ngyuen at Wilsonville

Activity: Peer Evaluation.

Rubric: Student evaluation survey were conducted by team members on other team members. Also a paper on leadership and teamwork was assigned. See appendix for sample submission of the Student Evaluation which students used to grade one another. Also, a tally of scores is provided. Papers on leadership/teamwork/lessons learned can be provided upon request. See Appendix E and F.

Sample and Reliability: Nine student artifacts assessed. Limited sample size may skew results. Scoring was performed by faculty of record for CST 372/373.

Multiple Sites: Terminology used in assignments are different but same content was covered.

Performance Target: Achieve grade of > 75% original requirements completed.

Performance Level:

Item		ESET	CET
1	Project Final Status Memo (% requirements complete)	100% (9/9)	N/A

History of Results: Not Available.

Faculty Discussion: All team members of all three groups graded all other team members > 75%. Also, papers were overwhelmingly positive.

Interpretation: Data provided in this report indicates that the Program Student Learning Objectives are being met for Wilsonville. Might include professor evaluations of team members next time.

Assessment K – KF - 473 - Direct

Learning Outcome: A commitment to quality, timeliness, and continuous improvement.

Course/Event: CST 473

Level: Capstone

Assessor & Campus: Kevin Pintong at Klamath Falls

Activity: Two papers were assigned. One paper was a test plan and the other paper was the final project document submissions.

Rubric: See Appendix B for grading rubric

Sample and Reliability: Ten student artifacts assessed. Limited sample size may skew results. Scoring was performed by faculty of record for CST 471.

Multiple Sites: Terminology used in assignments are different but same content was covered.

Performance Target: Achieve grade of > 80% according to rubrics for each item.

Performance Level:

Item		ESET	CET
1	Score from grading rubric for final report above 80%	67% (2/3)	67% (4/6)
2	Score from grading rubric for test plan above 80%	33% (1/3)	67% (4/6)

History of Results: Not Available.

Faculty Discussion: Results are discussed in next cycle.

Interpretation: While the limited sample size is not helpful, there are several reasons to explain the low performance. Some students received job offers which made them decide to do the bare minimum to graduate.

Students also frequently have a difficult time completing the project and test plan in time. For this reason, instructor will consider starting on project in CST 471 sooner. This indicates that an improvement can be made. Improvement and action plan discussed in Section 7.

Assessment K – WL - 473 - Direct

Learning Outcome: A commitment to quality, timeliness, and continuous improvement.

Course/Event: CST 473

Level: Capstone

Assessor & Campus: Phong Ngyuen at Wilsonville

Activity: A paper on quality and continuous improvement was assigned and graded to a rubric

Rubric: See Appendix J for grading rubric

Sample and Reliability: Four student artifacts assessed. Limited sample size may skew results. Scoring was performed by faculty of record for CST 471.

Multiple Sites: Terminology used in assignments are different but same content was covered.

Performance Target: Achieve grade of > 80% according to rubrics for each item.

Performance Level:

Item		ESET	CET
1	Score from grading rubric above 80%	100% (4/4)	N/A

History of Results: Not Available.

Faculty Discussion: Results are discussed in next cycle.

Interpretation: Data provided in this report indicates that the Program Student Learning Objectives are being met for Wilsonville. Limited sample size.

Assessment K – KF - 373 – Direct

Learning Outcome: A commitment to quality, timeliness, and continuous improvement.

Course/Event: CST 373

Level: Capstone

Assessor & Campus: Mike Healy at Klamath Falls

Activity: A paper on specific design improvements was assigned and graded to a rubric.

Rubric: See Appendix H for grading rubric

Sample and Reliability: Four student artifacts assessed. Limited sample size may skew results. Scoring was performed by faculty of record for CST 373.

Multiple Sites: Terminology used in assignments are different but same content was covered.

Performance Target: Achieve grade of > 80% according to rubrics for each item.

Performance Level:

Item		ESET	CET
1	Score from grading rubric above 80%	94% (9/13)	94% (4/13)

History of Results: Not Available.

Faculty Discussion: Specific feedback on content is given prior to submission. Results are kept in file for discussion during final exam week and beyond to next cycle.

Interpretation: Data provided in this report indicates that the Program Student Learning Objectives are being met for Klamath Falls.

Assessment K – WL - 372 and 373 – Direct

Learning Outcome: A commitment to quality, timeliness, and continuous improvement.

Course/Event: CST 372/373

Level: Capstone

Assessor & Campus: Phong Ngyuen at Wilsonville

Activity: A paper on quality and continuous improvement was assigned and graded to a rubric

Rubric: See Appendix J for grading rubric

Sample and Reliability: Three student artifacts assessed. Limited sample size may skew results. Scoring was performed by faculty of record for CST 372/373.

Multiple Sites: Terminology used in assignments are different but same content was covered.

Performance Target: Achieve grade of > 80% according to rubrics for each item.

Performance Level:

Item		ESET	CET
1	Score from grading rubric above 80%	100% (4/4)	N/A

History of Results: Not Available.

Faculty Discussion: Results are discussed in next cycle.

Interpretation: Data provided in this report indicates that the Program Student Learning Objectives are being met for Wilsonville. Limited sample size.

Section 7 – Data-driven Action Plans: Changes Resulting from Assessment

Improvements in Assessment Process:

- **Current Cycle (2018-2019):**
    - We re-designed three year assessment cycles for PSLOs around new ABET ETAC 1-5 requirements and identified faculty who will collect data.
    - We discussed data collected from the previous cycle (2017-2018) in our meeting and determined that we need to collect more detailed data on assignments, and provide better assignment descriptions to show that our students are meeting the PSLO.
    - Our dataset for this cycle has been dramatically improved. We have more supporting documentation. Our improvement in coordination between campuses yielded much more standardized and reliable data set between campuses.

- **Future (2019-2020):**
    - We need to make sure that courses between both campuses have alignment in course learning outcomes and PSLOs. Our new curriculum map shows the new PSLOs for this cycle. With George Drouant and Pramod Govindan hired to replace faculty who left or retired, we need to make sure courses are in alignment.

Action Plan for 2019-2020

Action Driver 1 : Assessment data for CST 471/473 – Outcome K.
Action Specifics 1 : Kevin Pintong will modify CST 471/472/473 for more development time in CST 471 in the 2019-2020 school year. Many students do not have sufficient time to complete test plans and reports in CST 473 because they are still finishing their project.
Reassessment: This outcome will not be reassessed per the ABET ETAC changes for the 2019-2020 cycle.

Action Driver 2 : General assessment activity
Action Specifics 2 : Kevin Pintong will review program courses to make sure courses are well-aligned.

Section 8 – Closing the Loop: Evidence of Improvement in Student Learning.

No data from previous cycle needed to be re-assessed.

Section 9 – Contact

Program Director:
Troy Scevers

Assessment Coordinator:
Kevin Pintong

Data provided by:

Michael Healy
Phong Ngyuen
Kevin Pintong
Office of Academic Excellence

Section 10 – Appendix A

Assessment A – WL CST 371 and CST 471

Rubric for project plan

	Highest level of competence
Timely submission	7 pts: final plan submitted by 5:00 pm, Friday of 10th week
Format/Organization	8 pts: inside folder, typed, double space, cover page, table of content, list of figures, list of lables, dividers separating each section
Spelling errors	5 pts: each spelling error incurs 1 pt off up to total of 5 pts
Grammatical errors	5 pts: each grammatical error incurs 1 pt up to a total of 5 pts
Modules	10 pts: break entire design into sensible, smaller modules. Examples of good modules are power supply, transmitting module, receiving module, output module, control module…
Hierarchichal design diagrams	10 pts: modular block diagrams broken down to top-level diagram which is in turn divided into smaller sub-level diagrams that describe clearly the modules of project. Each block diagram will be backed up by a detailed wiring schematic.
Diagram explanation	20 pts: provide precise write-up/explanation of each diagram. Any assembler without deisgn knowledge should be able to read the diagrams and explanation and be able to assemble the device.
Test Plan	15 Pts:Provide a step by step test plan broken down to plan for each sub-modules, modules, module integration and final product test.
Update parts list/commitment to certain percentage of variation preliminary list	5 pts: provide updated parts list (wish list). Annotate parts that the team has in hand. Prof. N will insist on seeing and touching ALL parts of parts list to compare with parts list. 20% off for each missing major part (microcontroller, PLD, input, output, power supply...)
Software requirements	10 pts: provide UML or flow charts of ALL software to be used. Must have written at least 20% of actual source code. Any hardware sophomores should be able to read your software requirements and proceed with ease to complete all source code of the project.
Preliminary cost	5 pts: estimated total cost. Estimated parts/packaging cost, engineering cost, labor cost, outsourced contract cost... Tabular format. Clear explanation of basis for estimation. Provide and explain estimated errors of estimated cost.
Team assignment	5 pts: Identify assigments/responsibilities of each
Rubric for project schedule	
	Highest level of competence
Timely submission	5 pts: final schedule submitted by 5:00 pm, Friday of 10th week
Format/Organization	10 pts: inside folder, typed, double space, formatted in some timeline fashion
Spelling errors	5 pts: each spelling error incurs 1 pt off up to total of 5 pts
Scheduled dates for start and receipt of major parts purchased	10 Pts: major parts examples are microcontroller, wireless, power supply… Do not worry minor parts like wires, headers...

Actual dates for start and receipt of major parts purchased	10 Pts: annotate when parts were actually purchased and received in order to compare
Schechuled dates for start and completion of each schematic in plan	10 pts: shedule for work on schematic of each module. Apart from minor testing, try not hook up hardware until schematic is done.
Scheduled dates for hardware and software start and completion of each module as specified in plan	10 Pts: once schematic and flow chart/UML are completed, wiring and coding must be scheduled
Scheduled dates for integration of modules. Be as detailed as possible on this part	10 Pts: schedule this keeping in mind the requirement that modules must be finished and tested indivually before integration
Scheduled dates for individual testing of major parts	10 Pts: make sure these dates are coordinated with testing of modules
Scheduled dates for testing of each module and integration of all modules	10 Pts: coordinate this with arrival of parts and testing of integration and final testing
Annotate who are the primary and secondary parties responsible for which part, which module, which testing	10 Pts: self explanatory
Rubric for control	
	Highest level of competence
Timely submission	5 pts: by 5:00 pm of Friday, 10th week
Format/Organization	5 pts: typed, double space in some formatted fashion
Spelling errors	5 pts: each spelling error incurs 1 pt off up to total of 5 pts
Grammatical errors	5 pts: each grammatical error incurs 1 pt up to a total of 5 pts
Firing of a group member	10 pts: Prof. N has a control measure for firing of a group member. What is the group's control measure before taking it up with the big N?
Habitual absence in meeting	10 pts: how many meetings can a member miss? What if someone misses too many meeting?
Missing deadline in ordering parts	10 pts: how does one track if someone has ordered parts or not? Having a schedule does not allow one to assume that responsible parties will follow schedules. If an ordering deadline is found to be missed what will be done to get the parts on time? What will become of the responsible parties?
Parts not arriving by scheduled arrival date	5 pts: whether parts are late due to late ordering or irresponsible vendors or long delivery time, one still must have parts by scheduled receipt date. What happens if parts does not arrive on time? What can be done, who will do it?
Module schematic delay	10 pts: what happens if schematic of each module is delayed? How much time can it be delayed? What happens if someone has to take over? Who will take over if it comes to that?
Module hardware and software delay	10 pts: What happens if the hardware and software are not completed for a module for whatever reasons? What possible reasons could cause delays: bad schematic, parts, interface…? Account for all possible delays!
Module integration delay	10 pts: What if all modules cannot be integrated by scheduled date? Identify all possible reasons for delays and actions that must be taken to alleviate the situations!

Annotation on schedule of ALL delays/problems	10 pts: how will you update the initial schedule if there are delays? DO NOT simply word process the schedule so that years from now it looks like no delays/problems took place. Find a way to annotate the schedule to show in details all problems and actions taken.
Firing of Prof N	5 pts: what if the person responsible for failure of project is big N. Be serious about this! If it is, what measures will you take!

Appendix B

Assessment A – KF CST 473

	Project Final Status Memo	Timely Completion	Project Final Report	Test Plan
Cpe Student 1	92.65	100	100	100
CpE Student 2	95	100	100	95
CpE Student 3	100	100	95	100
CpE Student 4	92	100	90	73
CpE Student 5	0	0	0	0
Cpe Student 6	63	100	72.5	67
ES Student 1	83.75	100	64.5	64.5
ES Student 2	97	100	90	90
ES Student 3	79	100	92.5	85

Test Plan Grading Rubric (Appendix B)

Test plan grading rubric			Include?	Possible
Introduction			1	10
System Block diagram			1	10
3.1	b	Software Requirements	1	10
	c	Explanation on how each requirement and corresponding subrequirement has been met through a specific test you developed. Data is shown and included in plan	1	20
	d	Provide a chart of how code is structured/organized. Your choice on diagram (Block diagram, flow chart, ASM, UML, State machine, etc.)	1	10
	e	List all tools used to generate the code. Compliers, synthesizers, IDEs, etc. It is important to indicate the exact version of each piece of software. Also list all external code you may have used such as libraries, API, etc.	1	10
	f	Notate any external code that you have used on this project.	1	5
	g	Provide a listing of all functions with declaration, input, return types, and possible failure conditions, and how the function was/will be tested.	1	10
	h	Timing if applicable	0	10

	i	RTL diagrams if applicable	0	10
3.2	a	Hardware requirements	1	10
	b	All hardware used- debuggers, IDE, synthesizer, oscilloscope, function generators, chips, etc. Make sure to write down serial numbers and model numbers.	1	10
	c	Explanation on how each requirement and corresponding subrequirement has been met through a specific test you developed. Data is shown and included in plan.	1	20
	d	Provide a picture of how the hardware is organized. This may also be your schematic.	1	10
	e	If you are using an ADC system, indicate that the ADC used consistently meets requirements of the system.	0	10
	f	If interfacing between different chips, screenshots proving that timing is within specification of the chips and that the clock speed is what was stated in report. You must include oscilloscope screenshots of rise time, fall time, and an overview for a data signal as well as control path signal for each external component you chose. Logic Analyzer is not acceptable for this purpose.	1	10
	g	Screenshots of digital bus signals indicating that the data sent and received from each component is correct. (Logic Analyzer is acceptable for this purpose.	1	10
	h	Notate any glitches you find in any I/O signal. It is acceptable to have glitches,but you must explain the scenario including probable cause. Make sure that you explain the expected value per specifications vs your received value.	1	10
	i	For projects with a power component, you must provide a detailed power budget for each component(average, peak, and quiescent voltage,current,power) and verify that at maximum load, the system will not exceed the power capabilities of the power supply. You must also indicate the efficiency of your power solution, battery life(if applicable). If hardware was built, indicate filtering circuitry such as high or low pass filtering and decoupling capacitors. Also provide a screenshot of power line to indicate the Vpp ripple.	0	10
3.3	a	Indicate available processor/SoC/FPGA and memory resources of your system (ROM, RAM, Logic Elements etc.)	1	10
3.4		Conclusion and areas of concern. Reflect on project improvements with respect to schedule, time, testing, etc.	1	10

Final report rubric CST 471 (Appendix B)

Evaluation	Comments	Valuation
Requirements	Requirements matrices and other requirements information is provided. Must explain how requirements are met.	15
Progress	Final product meets requirements and is functional	75
Depth of content	Report contains enough explanations, resources, and references such that another competent engineer could quickly understand and work on your project.	15
Accuracy of content	Technical statements made are accurate and described in an easy to understand manner.	15
Included content	Report must contain the following: Updated timelines including projected testing timeline NRE costs Firmware and software (Minimum of the module or function declarations, if used) Hardware schematics, layout (If used) Simulations (If used) Algorithms, protocols, must be included. They do not need to be mentioned in detail, but enough details about your specific implementation should be included (Example- SPI clock polarity choice) Conclusion indicating whether the project was successful and deviations made from original plan. For testing, refer the reader to the assurance plan which you will include in the appendix. Include the memos and other documentation generated through the previous three terms as well. Include lessons learned from your project. What would you have done differently?	40
Report organization	The report is organized in such a way that it is easy to navigate. Large sections of code or other large items are placed in Appendix. Smaller items are scattered throughout report with proper references. Report must contain introduction, abstract, conclusion, and main body of report organized into sections appropriate for your project.	10
Word choice, grammar, sentence structure	The report is free of first person references aside from included Memos and other documents. The report has proper word choice, grammar, and sentence structure.	10
References	Information in report, figures, diagrams, images, etc. are properly cited	10
	Information taken from datasheets is properly cited	5
	IEEE standard must be used for referencing	5
	Total possible points	200

Appendix C

Assessment A – KF CST 371

Project Plan Rubric

The purpose of this document is to describe the requirements and grading criteria for your project.

Timely submission:
7 pts - Submit by 5:00 pm, Friday of 10th week. 2 pts deducted for each day late.

Format/Organization:
8 pts – Word processed / double spaced. Include a cover page, page numbers, a table of contents, list of illustrations, and list of tables. Use headings for each section.

Note: As with the Proposal**, e**lectronic submittals are okay. If you choose to turn in a paper submittal, it should appear professionally prepared. Use a report cover or a binder.

Spelling and Punctuation:
5 pts - Each spelling error incurs 1 point off up to total of 5 points.

Grammatical errors:
5 pts - Each grammatical error incurs 1 point up to a total of 5 points.

Break down into modules / Subassemblies:
10 pts – Break down the entire design into smaller, manageable modules, and describe what each does. Examples of good module segmentation would be power supply, transmitting module, receiving module, output module, control module, etc.

Hierarchical design diagrams \ Schematics (Wiring Diagrams)
20 pts – Several block diagrams that reflect the modular breakdown described in the previous section, as well as an ordered task breakdown (fundamental tasks on the bottom). Remember, even your algorithms can be expressed in a hierarchical structure. Begin with a single top-level and divide into smaller scoped sub-levels. Clearly describe each individual block. Block diagrams and schematics are not the same thing - provide both! Draw a schematic for each of the wired segments that you will need to build or integrate. Once again, these should be broken down into manageable segments. The breakdown for individual schematics will likely be reflective of your block diagram structure and organization.

Detailed diagram descriptions:
10 pts - Provide precise explanations *for each diagram and schematic*. At this point consider that an assembler - someone without prior knowledge of your design – should be able to read the diagrams and explanations, and then perform the wiring or assembly.

Test plan:
15 pts - Provide step by step test plans, broken down by modules and sub-modules, down to the level of test plans for individual components. You want to verify proper operation of each part, especially for parts that are more complex and costly (e.g., the microcontroller, or the power supply). Insure this is all done *prior to* integration. Include test plans for module level integration as necessary (module-by-module). And then finally, provides details on how you plan to test your final assembled product.

Update your parts list, and your commitment to the percent variation that was expressed in your proposal:
5 pts - Provide an updated parts list and annotate which parts the team may already have on hand. I will ask to see whatever parts you have on hand before the break, and I will compare what I see with this list. Points off for major parts that have not been identified. Major parts include, for example, the microcontroller, PLD, i/o components, or power supply. Remember, all parts must be either on order or specified and ready to be ordered by the end of the 10th week of the fall term. This was expressed in the Project Selection Criteria you received early fall term.

Software specification:
10 pts – Provide a written software specification that describes the functional requirements of each and every software module that's to be used or created for your project. Provide as much detail as possible and include UML, flow charts, state diagrams, data management structures, or any design tools you are using to describe the flow of data. Again consider that any CSET sophomore should be able to read your software requirements and then write all of the source code for your project with minimal guidance. Be specific and comprehensive. Furthermore, understand that by the end of the term, all pseudo code should be written and you should expect to have at least 20% of your actual source code finished.

Individual team member assignments:
5 pts – Identify the assignments and responsibilities for each team member within the context of the project.

Project Schedule Rubric

This document describes the requirements and grading criteria for your **project schedule** submission. Each of the items is accompanied by certain number of points. Please note the *definite dependencies* that exist between buying parts, parts testing, your build, module testing, module integration, and final testing. This is the reason you will want to consider a Gantt-type approach.

Timely submission:

5 pts - Submit by 5:00 pm, Friday of 10th week.

Format/Organization:

10 pts – Typed and double spaced, **or tabular**. The format should be arranged into some *reasonable* timeline fashion: an hourly timeline would be excessive / *some* monthly milestones maybe, but monthly task updating would be insufficient. Include page numbers as appropriate.

Spelling errors:

5 pts - Spelling and punctuation errors incurs 1 point off up to a total of 5 points.

Include scheduled dates for order and receipt of major parts:

10 pts – Major parts and components would include, say, microcontroller, wireless transmitter/receiver, development board, power supply, etc. Minor parts like wires and headers don't really need to have their own entries on the schedule.

Actual dates for having ordered and received major parts:

10 pts – This section will provide a comparison for the baseline items above. Include dates that parts were *actually* ordered, paid for, and received. Annotate with reasons for deviations.

Schedule dates for testing of individual major parts:

10 pts – Make sure these dates are coordinated with the testing of modules as described in the section below.

Schedule dates for start and completion of each schematic listed in your plan:

10 pts – Include all schematics for each module. The completion date is important: Apart from minor testing, *try to not wire up your component hardware until* that particular schematic is finished. This may help you to avoid blowing things up.

Schedule dates for ALL hardware/software modules specified in your plan:

10 pts – This should be in accord with the work breakdown expressed in your plan. It needs to include *start and end* dates for flow charts, data flow representations, UML tools, and other tools. Then next, *as those tasks are completed*, wiring and coding should commence. Show scheduling start and end dates for these activities as well.

Schedule dates for testing of each individual module:
10 pts – Coordinate with the parts testing above, and with the integration and final testing items below.

Schedule dates for integration of modules and final test:

10 pts – Expect there to be multiple stages of integration, as well as a final test stage. You want to be as detailed as you possibly can on this part. Even though it is a bit far off in time, it's a very important look-ahead and significant milestone. Nearly all of your team's productive efforts will converge around these dates. Bear in mind that your modules must be finished and individually tested prior to integration. Integration itself will culminate in a final test of your fully integrated system.

Responsible team members (further development of team roles):

10 pts – Place the names of the responsible engineer(s) onto the schedule. Annotate who the personnel are that will be responsible for each part, each module, and each test. You may list more than one team member for each item; this may reflect a sub-team effort, or you may be indicating primary and secondary responsibility of team members. Make this distinction clear.

Naturally this requirement should draw on the individual team member assignments as outlined in your Project Plan.

Project Control Rubric

This document describes the requirements and grading criteria for your **project control** document. Your task with this document is to articulate how you will *monitor and control the progress of the project* through consideration of the items outlined below. You may include additional methods and ideas for how you plan to keep your project on track and moving forward over the course of the next seven months.

As with the planning and scheduling rubrics, you have until the final week of the fall term to craft this document. It's advised that you **don't try and complete this one until you've developed your planning criteria** and have worked out a schedule that comprehensively covers the outlined requirements. By working on this last, you're more apt to have developed a useful guideline for your team over the life of the project.

Timely submission:

5 pts - By 5:00 pm Friday, 10th week.

Format/Organization:

5 pts – Typed and double-spaced with page numbers.

Spelling/Punctuation errors:

5 pts - Each error incurs a 1 point deduction up to a total of 5 points.

Grammatical errors:

5 pts – Each grammatical error incurs a 1 point deduction, up to a total of 5 points.

Removal of a team member:

10 pts – I have established a control measure for the removal of a team member. What is the team's *internal* control measure before you would need to take it up with me? Define specific offenses. Agree on how best to discuss problems, giving ample opportunity for remedy in order to facilitate continued progress.

Habitual absences from meetings:

10 pts – How many meetings is a teammate allowed to miss? What happens if someone misses too many meetings? Discuss the implications and name the consequences.

Missing a deadline for ordering parts:

10 pts – How does one keep track of whether someone has ordered parts or not? Understand that having a schedule does not automatically insure that responsible parties will follow schedules. Remember that "responsible parties" include manufacturers and retailers. If an ordering deadline is found to have been missed, what can be done to still get the parts in on time? What are the consequences for the responsible parties? In other words, how do you fix the process and/or correct the behavior? Alternate suppliers, automated ordering triggers, secondary team member follow-up, etc.

Parts don't arrive by the scheduled arrival date:

5 pts – You still need to obtain the parts by the scheduled receipt date regardless of factors like delays in ordering, irresponsible vendors, or long delivery times. Furthermore, what happens if a part does not arrive on time? What can be done and who's going to do it?

Module schematic delay:
10 pts – What happens if the development of schematics for one or more modules is delayed? How much time can it be delayed by without having a detrimental effect on project development? Consider relative differences between a "serious level" and a "critical level" of impact. What happens if one team member cannot complete the schematic and someone else has to take over? Define how it's to be done. Which team member will fill the gap?

Module hardware and software delay:

10 pts – Likewise for hardware and software development: What happens if your hardware build or the software modules are not completed by the module test dates for any reason? Consider potential reasons that could result in delays: bad schematics, parts issues, circuit failure, etc. What else? *Consider and account for* possible delay scenarios.

Module integration delay:

10 pts – What if the modules cannot be integrated by the scheduled integration and test date? Identify possible reasons for these sorts of late-in-time delays, and consider actions that must be taken to recover.

Annotation of the schedule to reflect ALL delays/problems:

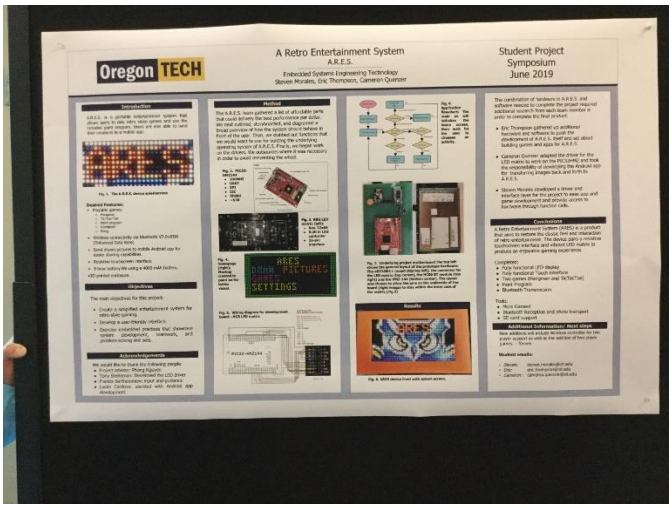
10 pts – How will you update the initial schedule you're developing this fall as you incur delays going forward in time? You SHOULD NOT simply alter a Gantt chart or a spreadsheet, or otherwise "word process" the schedule so it appears as if no delays or problems ever took place. That would make your schedule a fairly useless document.

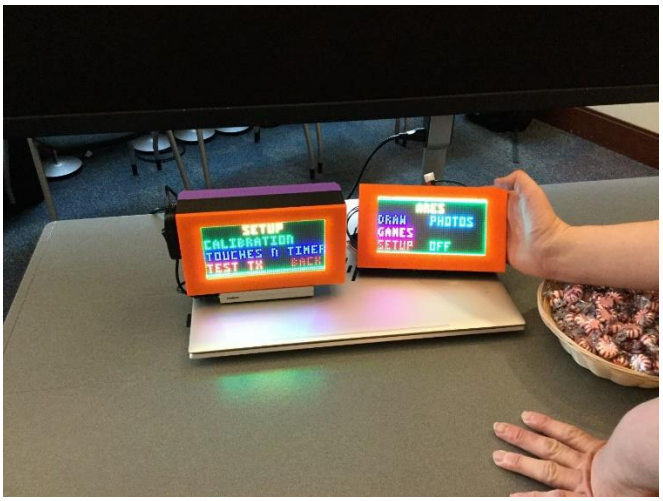
Develop and rely on some way to annotate your schedule showing *in detail* the problems that you are going to experience. These snares should then point to new actions on the schedule: actions you're going to take to overcome the issues in order to continue your progress.

Firing your professor:
5 pts – What if the person responsible for failure of the project is me, as your professor? Be serious about this! What if my advice leads you astray? What if I consume an inordinate amount of your time or in any other way I get in the way of your success? What measures will you take?

Appendix E

Assessment D – WL CST 371 and CST 471





Left to right: Cameron Quenzer, Steven Morales, Eric Thompson

Appendix F

Assessment E – WL CST 372/373

PEER EVALUATION Team Name: XXXXXXXXX **Evaluated**: A or B (yep circle A or B. Your teammate has been impersonalized to A or B)

Category **Grade**

1. Attitude (Motivation toward project, team members, customers. __10____
   Work ethics, positive/negative outlook on tasking)
2. Teamwork (Assists others, accepts assistance, respects opinions, __10____
   cooperates, resolves conflicts effectively, motivates others)
3. Workload (Assigned fair share, accomplishes assigned work, __10____
   willing to take on extra work to accomplish tasks)
4. Work quality (Completed work is of highest standard) __9____
5. Reliability (Accepts hard work, completes assigned work promptly __10____
   and effectively, accepts responsibility for work quality)
6. Communication (Listens to others, establishes clear expectations of __10____
   others, understand clearly written/verbal correspondence)
7. Time management (Attends all required functions, not procrastinate, __8____
   schedules work effectively, multitasks effectively)
8. Technical proficiency (Utilizes prior knowledge to design effectively) __10____
9. Ability to learn/improve/change/adapt __10____
10. Ability to document work (paperwork) __10____

TOTAL: __97____

COMBINED DATA

	Score a	b	c	d	e	f	g	h	i	Average
Attitude	10	10	10	10	10	10	10	8	9	9.666667
Teamwork	10	9	10	8	10	10	10	9	9	9.444444
Workload	10	10	3	8	10	10	10	9	10	8.888889
Work quality	9	9	10	10	10	10	10	10	7	9.444444
Reliability	10	9	5	10	10	10	10	10	8	9.111111
Communication	10	8	7	2	10	10	10	4	10	7.888889
Time manage	8	8	5	10	10	10	10	7	9	8.555556
Tech proficiency	10	10	10	10	10	10	10	7	8	9.444444
Improve/adapt	10	10	10	10	10	10	10	9	8	9.666667
Documentation	10	10	6	10	10	10	10	4	10	8.888889
TOTAL	97	93	76	88	100	100	100	77	88	91

Appendix G

Assessment E – KF CST 372/373

PEER EVALUATION

Team Name: [redacted]

Teammate Evalu [redacted]

INSTRUCTIONS: Grade each category on a 10-point basis with 10 being the best grade.

Category		Grade
1. Attitude	(Motivation toward the project, team members, and others. work ethic, positive / negative outlook on tasking)	8
2. Teamwork	(Assists others, accepts assistance, respect other's opinions, cooperates, resolves conflicts effectively, motivates others)	10
3. Workload	(Assigned a fair share, accomplishes assigned work, willing to take on extra work to accomplish tasks)	10
4. Work quality	(Completed work is of the highest standard)	10
5. Reliability	(Accepts difficult tasks, completes assigned work promptly and effectively, accepts responsibility for work quality)	10
6. Communication	(Listens to others, establishes clear expectations of others, understands clearly written or verbal correspondence)	8
7. Time management	(Attends all required functions, does not procrastinate, schedules work effectively, multitasks effectively)	9
8. Technical proficiency	(Utilizes prior knowledge to design effectively)	10
9. Ability to learn / improve / change / adapt		10
10. Capability toward documenting work (paperwork)		10
11. Have you enjoyed this teammate's leadership style?		9
12. Rate this teammate as a leader (During anytime that they served in this role)		10
13. How do you rate your own leadership in comparison to your teammate's	(Place your self-ranking of 1 to 10 here)	8

TOTAL: 122

COMMENTS (use additional sheets if necessary):

Appendix H

Assessment K – KF CST 373

Timely Submission:	5 pts - submit by 5:00 p.m. Friday of week 10.
Spelling & Punctuation Errors:	5 pts - each spelling or punctuation error will incur 1 point off, up to total of 5 points.
Grammatical Errors:	5 pts - each grammar error will incur a 1 point loss up to a total of 5 points.
Format and Organization:	5 pts – Use 12 point font. Double-spaced. Structure the document with an introduction, a body, and a conclusion. The length may vary, but I would expect to see at least a 6 to 8 page paper with a table of contents, references, and a list of figures. Paper or electronic submission is okay.
Appropriate Module Selection:	10 pts – Describe the candidate module for improvement in this introductory section. Make sure to choose a module or modules of your project that includes both software *and* hardware elements to improve upon. Ask yourselves if the proposed improvement adds value in some way (e.g., a feature that's desired and therefore worth adding, a reduction in fabrication cost, something that reduces operating costs for the user, something that has a secondary use or purpose, etc.)
Hardware Design:	10 pts – Discuss the necessary changes in the hardware design of the module. Implementing the improvement in hardware is likely to change the components in use. Add schematics and block diagrams as necessary and make sure to include these in this paper.
Software:	10 pts – Likewise for the software changes necessary to implement the improvement. Be specific. Include pseudocode and alterations to data flow as required.
Fabrication:	10 pts – Discuss how you will handle the necessary changes in how you would build a prototype. What will the improved system look like?
Hardware and Software Test:	10 pts – Discuss how you will test both hardware and software aspects of the improvement. Consider what testing criteria you will need: environmental, diverse system stimuli (input), expected outputs, testing bounds, etc. Consider your past testing experience (lessons learned) on this project and others.
Analysis and Interpretation:	10 pts – Go through the process of analysis and interpretation of test data. Perform the testing and provide results if you can. What assumptions, actions or recommendations resulted? This section can be far easier to write if you can systematize some kind of mock test, as opposed to attempting to formulate a series of hypothetical test projections. Do one or the other. If the latter method is invoked then *be sure* you take a comprehensive approach to cover the unknowns.
Improvements in General:	10 pts – Summarize *all improvements* made to your team's project over the course of the year. Include additional suggestions or improvements based on the results of the analysis done in the sections above.
Conclusion:	10 pts –Summarize the main points of your paper in order to provide a final word on the value of exploring this improvement.

Appendix I

Assessment K – KF CST 471

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Appendix J

Assessment K – WL CST 371 and 471

Rubric for paper is below.

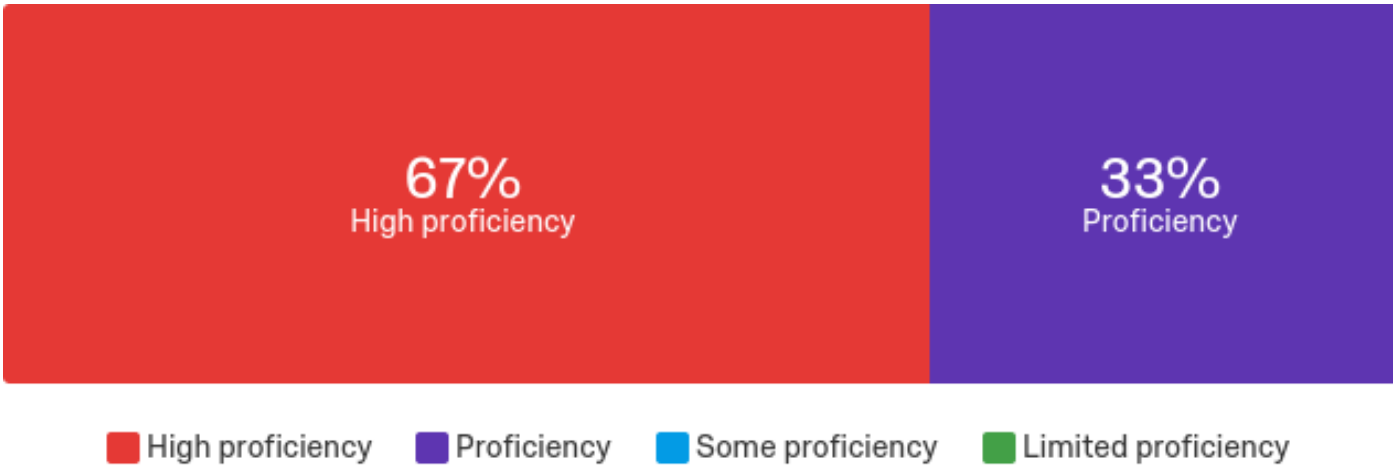
Name:	Rubric:	Lessons Learned		
	Explanation	Grader's Remark:	Pts Total	Pts Received
Prompt submission	By 5:00 pm, Friday, 10th week		5	
Spelling	1 pt off per error up to 5 pts		5	
Grammar	1 pt off per error up to 5 pts		5	
Format	12 pt font, double space, 4-5 pages, intro/body/conclusion		5	
Problem identification	Choose one major problem encountered during the design that caused major technical redesign, change in plan and schedule		10	
Technical	Discuss technical aspect of problem		20	
Plan	Discuss change of plan		15	
Schedule	Discuss change of schedule		15	
Lessons learned	Discuss major lesson learned. And provide suggested changes for future groups		20	

	Score from graded rubric
Team ARES	91
Team O2	92
Team Vent	90
Senior A	85
Senior B	88

Appendix K

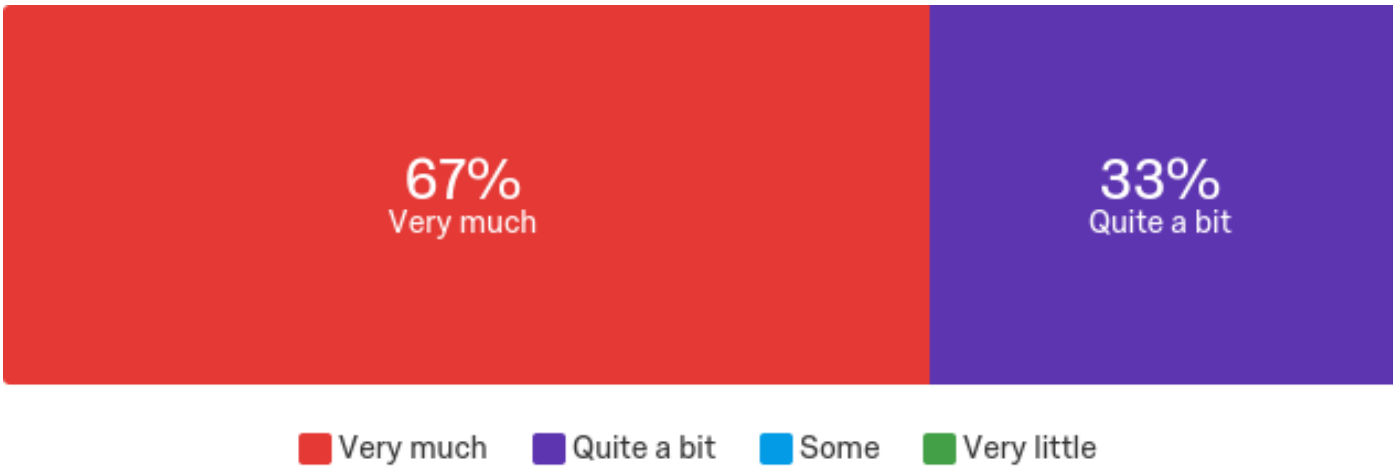
Indirect Assessment - Student Exit survey results

Q ESLO 1 - Oregon Tech Essential Student Learning Outcomes Please rate your proficiency in the following areas.



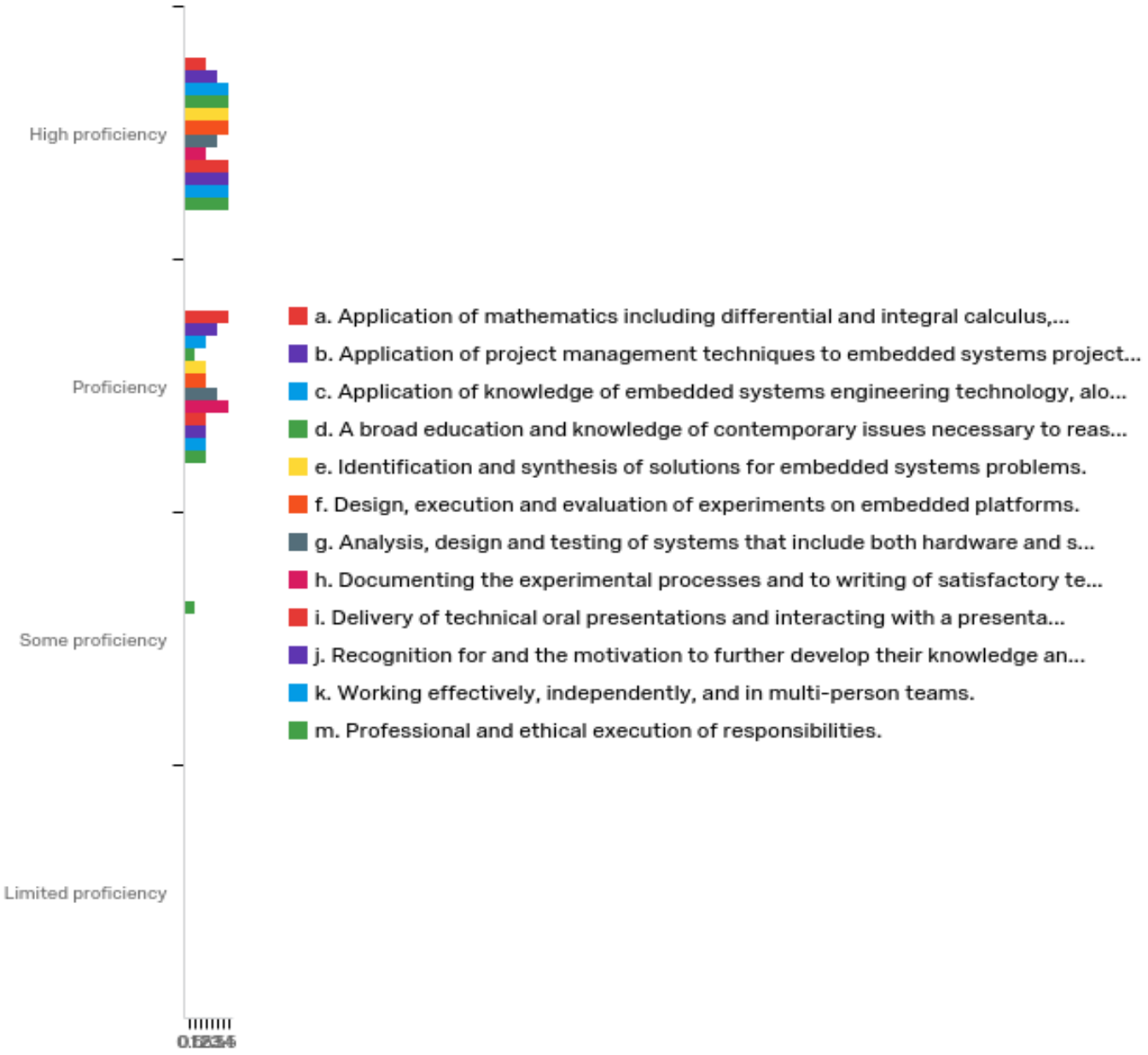
#	Question	High proficiency		Proficiency		Some proficiency		Limited proficiency		Total
1	ESLO 1a. Communication: Writing effectively	66.67%	4	33.33%	2	0.00%	0	0.00%	0	6
2	ESLO 1b. Communication: Speaking effectively	33.33%	2	66.67%	4	0.00%	0	0.00%	0	6
3	ESLO 2. Inquiry & Analysis: Thinking critically and analytically	100.00%	6	0.00%	0	0.00%	0	0.00%	0	6
4	ESLO 3. Ethical Reasoning: Making ethical judgements	66.67%	4	33.33%	2	0.00%	0	0.00%	0	6
5	ESLO 4. Teamwork: Work effectively with groups and teams	66.67%	4	33.33%	2	0.00%	0	0.00%	0	6
6	ESLO 5. Quantitative Literacy: Using quantitative/numerical information to solve problems, evaluate claims, and support decisions	83.33%	5	16.67%	1	0.00%	0	0.00%	0	6
7	ESLO 6. Diverse Perspectives: Understanding of diverse perspectives to improve interactions with others	83.33%	5	16.67%	1	0.00%	0	0.00%	0	6

Q ESLO 2 - Oregon Tech Essential Student Learning Outcomes How much has your experience at Oregon Tech contributed to your knowledge, skills, and personal development in these areas?



#	Question	Very much		Quite a bit		Some		Very little		Total
1	ESLO 1a. Communication: Writing effectively	66.67%	4	33.33%	2	0.00%	0	0.00%	0	6
2	ESLO 1b. Communication: Speaking effectively	66.67%	4	33.33%	2	0.00%	0	0.00%	0	6
3	ESLO 2. Inquiry & Analysis: Thinking critically and analytically	66.67%	4	16.67%	1	16.67%	1	0.00%	0	6
4	ESLO 3. Ethical Reasoning: Making ethical judgements	50.00%	3	33.33%	2	16.67%	1	0.00%	0	6
5	ESLO 4. Teamwork: Work effectively with groups and teams	66.67%	4	33.33%	2	0.00%	0	0.00%	0	6
6	ESLO 5. Quantitative Literacy: Using quantitative/numerical information to solve problems, evaluate claims, and support decisions	66.67%	4	33.33%	2	0.00%	0	0.00%	0	6
7	ESLO 6. Diverse Perspectives: Understanding of diverse perspectives to improve interactions with others	50.00%	3	33.33%	2	16.67%	1	0.00%	0	6

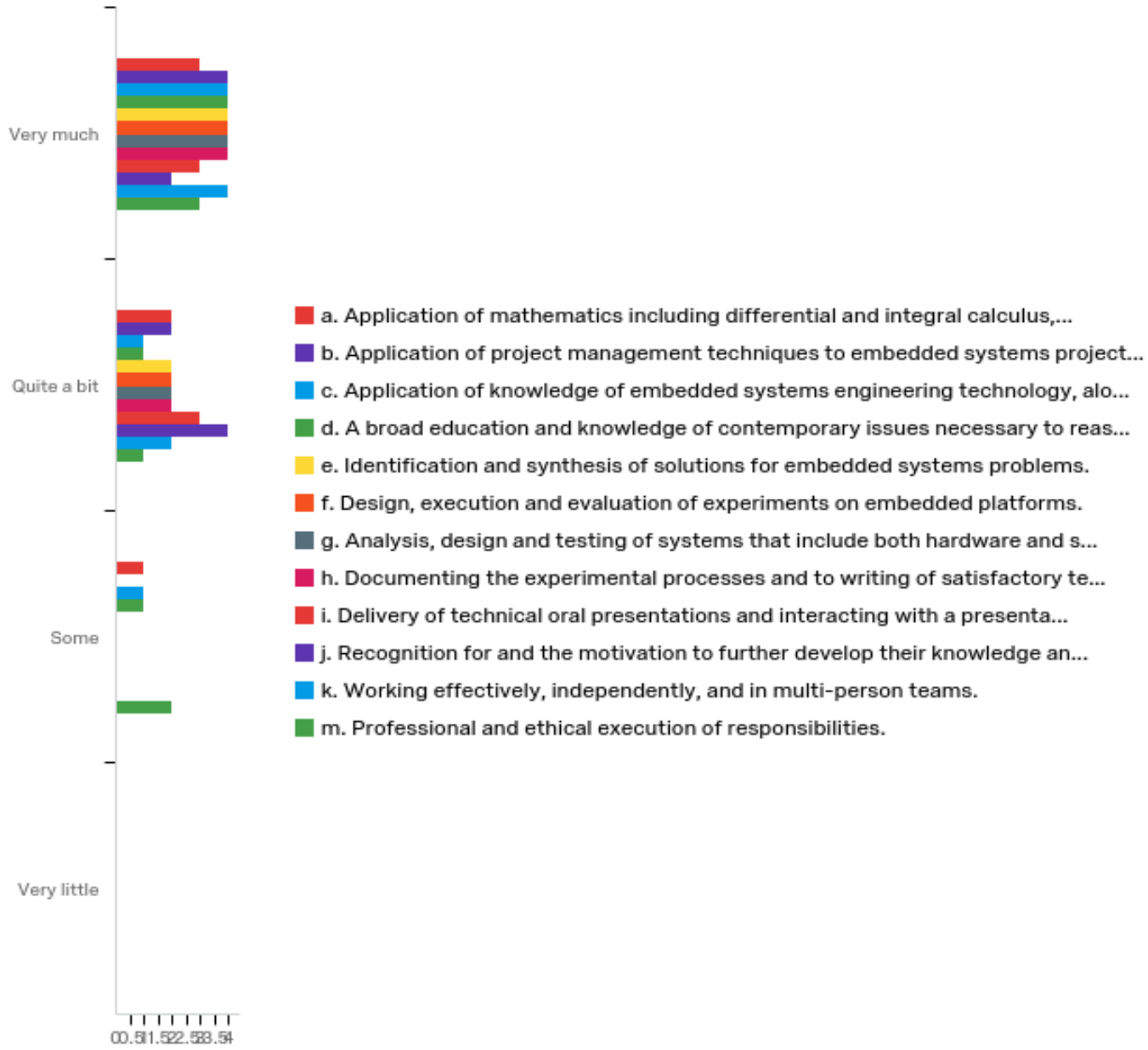
Q BEMB 1 - Program Student Learning Outcomes for Embedded Systems Engineering Technology B.S. Please rate your proficiency in the following areas.



#	Question	High proficiency		Proficiency		Some proficiency		Limited proficiency		Total
1	a. Application of mathematics including differential and integral calculus, probability, and discrete mathematics to hardware and software problems.	33.33%	2	66.67%	4	0.00%	0	0.00%	0	6
2	b. Application of project management techniques to embedded systems projects.	50.00%	3	50.00%	3	0.00%	0	0.00%	0	6
3	c. Application of knowledge of embedded systems engineering technology, along	66.67%	4	33.33%	2	0.00%	0	0.00%	0	6

	with some specialization in at least one area of computer systems engineering technology.									
4	d. A broad education and knowledge of contemporary issues necessary to reason about the impact of embedded system based solutions to situations arising in society.	66.67%	4	16.67%	1	16.67%	1	0.00%	0	6
5	e. Identification and synthesis of solutions for embedded systems problems.	66.67%	4	33.33%	2	0.00%	0	0.00%	0	6
6	f. Design, execution and evaluation of experiments on embedded platforms.	66.67%	4	33.33%	2	0.00%	0	0.00%	0	6
7	g. Analysis, design and testing of systems that include both hardware and software.	50.00%	3	50.00%	3	0.00%	0	0.00%	0	6
8	h. Documenting the experimental processes and to writing of satisfactory technical reports/papers.	33.33%	2	66.67%	4	0.00%	0	0.00%	0	6
9	i. Delivery of technical oral presentations and interacting with a presentation audience.	66.67%	4	33.33%	2	0.00%	0	0.00%	0	6
10	j. Recognition for and the motivation to further develop their knowledge and skills as embedded engineering advances occur in industry.	66.67%	4	33.33%	2	0.00%	0	0.00%	0	6
11	k. Working effectively, independently, and in multi-person teams.	66.67%	4	33.33%	2	0.00%	0	0.00%	0	6
12	m. Professional and ethical execution of responsibilities.	66.67%	4	33.33%	2	0.00%	0	0.00%	0	6

Q BEMB 2 - Program Student Learning Outcomes for Embedded Systems Engineering Technology B.S. How much has your experience at Oregon Tech contributed to your knowledge, skills, and personal development in these areas?



#	Question	Very much		Quite a bit		Some		Very little		Total
1	a. Application of mathematics including differential and integral calculus, probability, and discrete mathematics to hardware and software problems.	50.00%	3	33.33%	2	16.67%	1	0.00%	0	6
2	b. Application of project management techniques to embedded systems projects.	66.67%	4	33.33%	2	0.00%	0	0.00%	0	6

3	c. Application of knowledge of embedded systems engineering technology, along with some specialization in at least one area of computer systems engineering technology.	66.67%	4	16.67%	1	16.67%	1	0.00%	0	6
4	d. A broad education and knowledge of contemporary issues necessary to reason about the impact of embedded system based solutions to situations arising in society.	66.67%	4	16.67%	1	16.67%	1	0.00%	0	6
5	e. Identification and synthesis of solutions for embedded systems problems.	66.67%	4	33.33%	2	0.00%	0	0.00%	0	6
6	f. Design, execution and evaluation of experiments on embedded platforms.	66.67%	4	33.33%	2	0.00%	0	0.00%	0	6
7	g. Analysis, design and testing of systems that include both hardware and software.	66.67%	4	33.33%	2	0.00%	0	0.00%	0	6
8	h. Documenting the experimental processes and to writing of satisfactory technical reports/papers.	66.67%	4	33.33%	2	0.00%	0	0.00%	0	6
9	i. Delivery of technical oral presentations and interacting with a presentation audience.	50.00%	3	50.00%	3	0.00%	0	0.00%	0	6
10	j. Recognition for and the motivation to further develop their knowledge and skills as embedded engineering advances occur in industry.	33.33%	2	66.67%	4	0.00%	0	0.00%	0	6
11	k. Working effectively, independently, and in multi-person teams.	66.67%	4	33.33%	2	0.00%	0	0.00%	0	6
12	m. Professional and ethical execution of responsibilities.	50.00%	3	16.67%	1	33.33%	2	0.00%	0	6