2020-2021

Program Assessment Report

Computer Engineering Technology

**Section 1 – Program Mission and Educational Objectives**

**Oregon Tech Mission:**

Oregon Institute of Technology, an Oregon public university, offers innovative and rigorous applied degree programs in the areas of engineering, engineering technologies, health technologies, management, and the arts and sciences. To foster student and graduate success, the university provides an intimate, hands-on learning environment, focusing on application of theory to practice. Oregon Tech offers statewide educational opportunities for the emerging needs of Oregonians and provides information and technical expertise to state, national and international constituents.

**Core Theme 1: Applied Degree Programs**

Oregon Tech offers innovative and rigorous applied degree programs. The teaching and learning model at Oregon Tech prepares students to apply the knowledge gained in the classroom to the workplace.

**Core Theme 2: Student and Graduate Success**

Oregon Tech fosters student and graduate success by providing an intimate, hands-on learning environment, which focuses on application of theory to practice. The teaching and support services facilitate students’ personal and academic development.

**Core Theme 3: Statewide Educational Opportunities**

Oregon Tech offers statewide educational opportunities for the emerging needs of Oregon’s citizens. To accomplish this, Oregon Tech provides innovative and rigorous applied degree programs to students across the state of Oregon, including high-school programs, online degree programs, and partnership agreements with community colleges and universities.

**Core Theme 4: Public Service**

Oregon Tech will share information and technical expertise to state, national, and international constituents.

**Computer Engineering Technology Program Mission:** The mission of the Computer Engineering Technology (CET) bachelor's degree program in the Computer Systems Engineering Technology (CSET) Department at Oregon Institute of Technology is to provide an excellent education incorporating industry-relevant, applied laboratory based design and analysis for our students. The program is to serve a constituency consisting of its students, alumni, and employers in industry and government. Major components of the CET program's mission in the CSET Department are to:

* educate computer engineering technology students to meet current and future industrial challenges,
* promote a sense of scholarship, leadership, and professional service among our graduates,
* enable our students to create, develop, and disseminate knowledge for the applied engineering environment,
* expose our students to cross-disciplinary educational programs, and
* provide high tech industry employers with graduates in the computer engineering technology profession

**Mission Alignment:**

Our program is very hands-on and thus aligns with Core Theme 1. Our graduates are in high demand by the industries we support. This is evidence that we are aligned with Core Theme 2. The program features two years of project-based learning environment with junior project and senior project.

**Section 2 – Program Description and History**

**Program History**

In 1965, OIT was invited to join a Technical Education consortium sponsored by a number of major computer manufacturers. In response, OIT developed an Electro-Mechanical Engineering Technology program. This program was based on a mix of existing EET, MET, Math and other support courses. The name of the program was changed to Computer Systems Engineering Technology in 1973 in order to better represent the course material and capabilities of graduates. Course offerings were expanded, refined and renumbered using CST prefixes to reflect their computer systems content. Since that time, the program has continued to evolve in order to track new developments in the field and keep graduates current. As of this time, the program is only offered on the Klamath Falls campus. The program has continuously evolved as industrial changes have warranted.

**Program Enrollment**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Campus** | **Fall 2015** | **Fall 2016** | **Fall 2017** | **Fall 2018** | **Fall 2019** | **Fall 2020** |
| Klamath Falls | 78 | 57 | 60 | 57 | 52 | 39 |
| Portland-Metro | 8 | 6 | 2 | 4 | 4 | 0 |
| Totals | 96 | 63 | 62 | 61 | 58 | 39 |

As of Fall 2020, enrollment in the Computer Engineering Technology program continues to see a decline. At least some of the drop can be attributed to Covid-19. Note that the program is only located on the Klamath Falls campus. The “Portland-Metro” line in the table above shows CET students on the Portland-Metro campus that are finishing their degree at that campus.

Faculty from Computer Engineering Technology, Embedded Systems Engineering Technology, Software Engineering Technology, and Electrical Engineering concur that correctly re-branding this program to Computer Engineering would improve enrollment. However, a number of issues, including Covid-19 and lack of upper administration approval have prevented this from coming to fruition.

**Program Graduates**

Graduate numbers for Computer Engineering Technology have remained relatively flat. Note again that there is no Computer Engineering Technology program on the Portland Metro campus, but students may be finishing their degree at that location.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **2015-16** | **2016-17** | **2017-18** | **2018-19** | **2019-20** | **2020-21** |
| 3 | 6 | 3 | 7 | 6 | 5 |

**Employment Rates and Salaries**

Institutional data indicates that graduates of the Computer Engineering Technology program are successful in finding employment. Some recent employers include 3DSystems Corp., DW Fritz, Garmin, Intel Corporation, and Hamilton. Some graduates are also pursuing graduate degrees in a related field.

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | % Employed | | | % Continuing Ed | | | Median Salary | | |
| a | b | c | a | b | c | a | b | c |
| **Computer Engineering Technology** | **100** | **93** | **88** | **0** | **7** | **13** | **64,000** | **65,500** | **64,000** |
| Embedded Systems Engineering Technology | 88 | 75 | 92 | 13 | 13 | 0 | 60,000 | 60,000 | 60,000 |
| Software Engineering Technology | 93 | 89 | 93 | 0 | 1 | 0 | 65,000 | 67,000 | 69,500 |

a = data from 2015 / 2016 / 2017 combined,   
b = data from 2016 / 2017 / 2018 combined,   
c = data from 2017 / 2018 / 2019 combined

Data are derived from a comprehensive survey of graduates, approximately six months post-graduation. It includes outcomes reported by graduates, faculty outreach and LinkedIn information. More information regarding the data used is available from Oregon Tech’s Career Services.

**Program Changes**

Kevin Pintong left at the end of June 2021 and Pramod Govindan left at the end of June 2020. Searches for their replacements have not been successful to date but are ongoing.

**Core Program Faculty**

|  |  |  |
| --- | --- | --- |
| George Drouant  George Drouant, Instructor (KF) | Michael Healy  Michael Healy, Assistant Professor (KF) | Dr. Douglas Lynn  Douglas Lynn, Professor (KF) |
| Phong Nguyen  Phong Nguyen, Assistant Professor (PM) | Troy Scevers  Troy Scevers, Program Director Embedded Systems Engineering Technology, Associate Professor (KF) |  |

**Section 3 – Program Student Learning Outcomes**

Graduates of the Computer Engineering Technology (CET) Bachelor Degree program may be employed in a wide range of high tech industries from industrial manufacturing to consumer electronics where they will be involved in solving problems through the development of hardware, software and embedded applications. Graduates may be involved in product design, testing and qualification, application engineering, customer support, sales, or public relations.

**Program Educational Objectives**

The Program Educational Objectives reflect those attributes a student of the CET program will practice in professional endeavors.

* Demonstrate technical competency through success in computer engineering technology positions and/or pursuit of engineering or engineering technology graduate studies if desired.
* Demonstrate competencies in communication and teamwork skills by assuming increasing levels of responsibility and leadership or managerial roles.
* Develop professionally, pursue continued learning, and practice computer engineering technology in a responsible and ethical manner.

**Program Student Learning Outcomes**

(1) an ability to apply knowledge, techniques, skills and modern tools of mathematics, science, engineering, and technology to solve broadly-defined engineering problems appropriate to the discipline.

(2) an ability to design systems, components, or processes meeting specified needs for broadly-defined engineering problems appropriate to the discipline.

(3) an ability to apply written, oral, and graphical communication in broadly-defined technical and non-technical environments; and an ability to identify and use appropriate technical literature.

(4) an ability to conduct standard tests, measurements, and experiments and to analyze and interpret the results to improve processes.

(5) an ability to function effectively as a member as well as a leader on technical teams.

**Program Student Learning Outcomes Update**

On September 18, 2020, the ESET and CET faculty met to review the mission statement, and program student learning outcomes. No changes were made as a result of these discussions. Faculty also met to discuss PSLO responsibilities for the 2020-2021 cycle, as assessment results for the 2019-2020 cycle.

**External validation**

External validation of PSLOs are achieved through the following:

1. Industry Advisory Board discussions
2. Graduate job placement and continuing education rates
3. ABET ETAC accreditation process

On Nov 20 2020, the mission statements and program student learning outcomes were presented to and approved by the department’s Industrial Advisory Board.

**Section 4 – Curriculum Map**

## Program Student Learning Outcome Coverage by Course

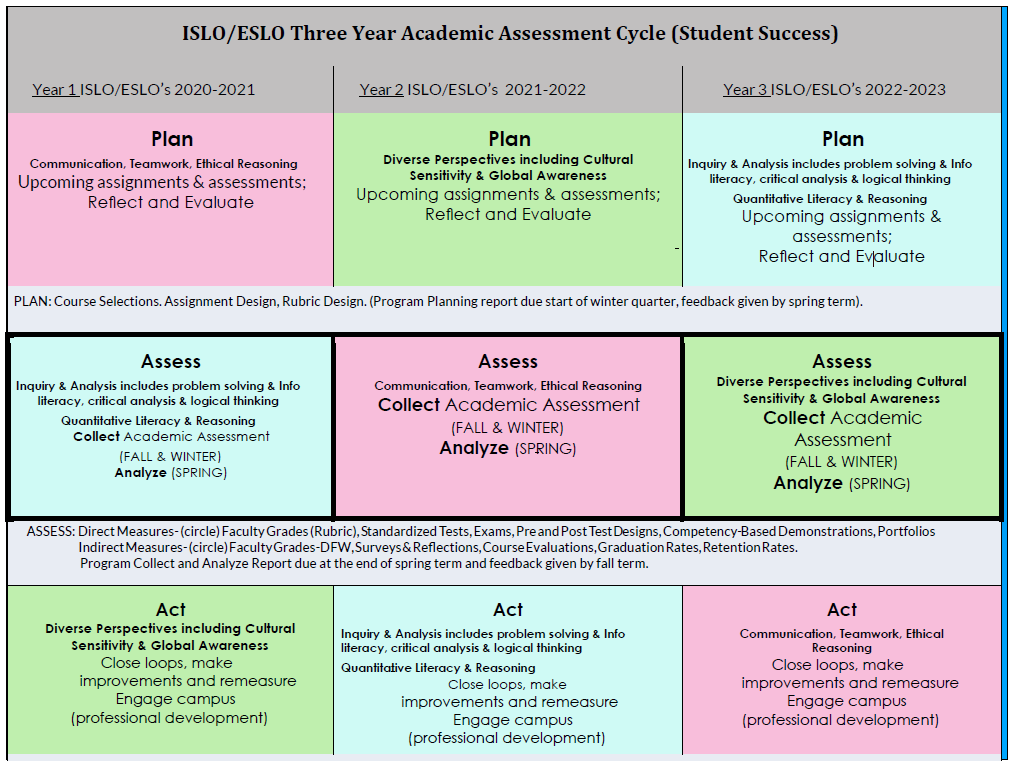
|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Course | Major | Title | PSLO | | | | |
| 1 | 2 | 3 | 4 | 5 |
| CST 162 |  | Digital Logic I | X |  |  |  |  |
| CST 130 |  | Computer Organization | X |  |  |  |  |
| CST 120 |  | Embedded C | X |  |  |  |  |
| CST 131 |  | Computer Architecture | X |  |  |  |  |
| CST 133 |  | Digital Logic II | X | x |  |  |  |
| CST 134 |  | Instrumentation | X |  |  | X |  |
| CST 250 |  | Computer Assembly Language | X | x |  |  |  |
| CST 204 |  | Introduction to Microcontrollers | X | x | x |  |  |
| CST 231 |  | Digital Systems Design I | X |  | X |  |  |
| CST 337 |  | Embedded System Architecture | X | X | x | X |  |
| CST 315 |  | Embedded Sensor Interfacing & I/O | X |  |  | X |  |
| CST 374 |  | Embedded Project Proposal | X |  | X |  |  |
| CST 371 |  | Embedded Systems Development 1 (Junior Project) | X |  | X | X | X |
| CST 372 |  | Embedded Systems Development 2 (Junior Project) | X |  | X |  | X |
| CST 373 |  | Embedded Systems Development 3 (Junior Project) | X |  | X |  | X |
| CST 471 |  | Embedded Senior Project 1 | X |  | X |  |  |
| CST 472 |  | Embedded Senior Project 2 | X |  | X |  |  |
| CST 473 |  | Embedded Senior Project 3 | X |  | X |  |  |
| CST 331 | CpE | Microprocessor Peripheral Interfacing | X | X | x | X |  |
| CST 418 | CpE | Data Comm & Networks | X |  |  |  |  |
| CST 351 | CpE | Digital System Design II | X |  | x |  |  |
| CST 344 | CpE | Intermediate Computer Architecture | X |  |  |  |  |
| CST 442 | CpE | Advanced Computer Architecture | X |  |  |  |  |
| CST 455 | ES | System on a Chip Design | X |  |  |  |  |
| CST 456 | ES | Embedded System Testing | X |  |  |  |  |
| CST 466 | ES | Embedded System Security | X |  | X | x |  |
| CST 417 | ES | Embedded Networking | X |  |  |  |  |
| CST 347 | ES | Real Time Embedded Operating Systems | X |  |  |  |  |

X = Major component, x = minor component

The curriculum map was last updated and approved on October 4, 2019. No curriculum or course content changes have been made since that time.

## Essential Student Learning Outcomes

Essential student learning outcomes are given in the table below at the introduction, practice, and capstone levels.



**Section 5 – Assessment Cycle**

The table below is the updated assessment cycle for 2020-2023. The assessment cycle below reflects changes made as a result of the ABET ETAC a-k to 1-5 learning outcomes change. PSLOs are assessed in a three year cycle and ESLOs are assessed in a six year cycle. Each PSLO will have two direct measurements (two classes) with one indirect measurement, and each ESLO will have one direct measurement.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **PSLO** | **ESLO** | **2020-2021** | **2021-2022** | **2022-2023** |
| (1) an ability to apply knowledge, techniques, skills and modern tools of mathematics, science, engineering, and technology to solve broadly defined engineering problems appropriate to the discipline; (ESLO Inquiry and Analysis) | Inquiry and Analysis | **CET/ESET: CST 162 (Phong)**  **CET: CST 442, 418 (Doug)**  **ESET: CST 456 (Stephen)** |  |  |
| (2) an ability to design solutions for well-defined technical problems and assist with the engineering design of systems, components, or processes appropriate to the discipline; |  |  |  | **CST 315  (George and Unknown)**  **CST 473 (Unknown Phong)** |
| (3) an ability to apply written, oral, and graphical communication in well-defined technical and non-technical environments; and an ability to identify and use appropriate technical literature; (ESLO Communication) | Communication |  | **CST 472 (Phong and Unknown)**  **CST 372 (Phong and Mike)** |  |
| (4) an ability to conduct standard tests, measurements, and experiments and to analyze and interpret the results; (ESLO Quantitative Literacy) | Quantitative Literacy | **ESLO**  **CET/ESET: CST 337 (Doug)**  **CET/ESET: CST 134 (George)**  **CET/ESET: CST 473 (Phong)** |  |  |
| (5) an ability to function effectively as a member of a technical team. (ESLO Teamwork) | Teamwork |  | **CST 371 (Mike, Phong)**  **CST 231 (Kevin, Unknown)** |  |
|  | Diverse Perspectives |  |  | **CST 471 (Kevin, Phong) ESLO Only**  **CST 371(Mike, Phong)** |
|  | Ethical Reasoning |  | **CST 472 (Phong and Unknown)**  **CST 372 (Phong and Mike)** |  |

**Section 6 – Assessment Activity**

This year’s assessment focused on the learning outcomes below.

Reference the following table and page numbers.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Assessment** | **Program Student Learning Outcomes**  **3-year cycle**  **Computer/Embedded Systems Engineering Technology B.S.** | **2020-2021** | **Page** | **Status** |
| **(1)**  **Inquiry and Analysis** | an ability to apply knowledge, techniques, skills and modern tools of mathematics, science, engineering, and technology to solve broadly engineering problems appropriate to the discipline; | **CET/ESET: CST 162 (Phong)**  **CET: CST 442, 418 (Doug)**  **ESET: CST 456 (Stephen)**  **Exit Survey** | **10**  **12 13**  **Not done**  **14** | **OK** |
| **(4)**  **Quantitative Literacy** | an ability to conduct standard tests, measurements, and experiments and to analyze and interpret the results; | **CST 337 (Doug)**  **CST 134 (George)**  **CST 473 (Phong)**  **Exit Survey** | **15**  **16**  **18**  **19** | **OK** |

**Assessment Level Key:**Foundation – introduction of the learning outcome, typically at the lower-division level,   
Practicing – reinforcement and elaboration of the learning outcome, or   
Capstone – demonstration of the learning outcome at the target level for the degree

**Assessment A – Wil - 162**

**Learning Outcome (1):** an ability to apply knowledge, techniques, skills and modern tools of mathematics, science, engineering, and technology to solve broadly defined engineering problems appropriate to the discipline;

**Course/Event:** CST 162 Direct Assessment

**Level**: Foundation

**Assessor & Campus:** Phong Nguyen at Wilsonville

**Activity**: Students are guided though the digital logic design of a Full adder (FA) using Verilog and implement it on a DE10 lite board. A series of benchmarks (see below) were used to assess each student’s understanding of basic logic design from the initial paper design through the final implementation and testing.

**Sample and Reliability**: Seven student artifacts were collected and assessed. Limited sample size may skew results. Scoring was performed by Phong Nguyen.

**Performance Target**: All steps of the design process should be successfully completed by 70% of students.

**Assessment Method**:

|  |  |  |
| --- | --- | --- |
| **Learning Objectives**  *What should students be able to do?* | **Learning Activities**  *How will students learn (assimilate, interpret, practice, and demonstrate) what is necessary to succeed on the assessments?* | **Assessments**  *What evidence would be acceptable to show that students have achieved the objectives?* |
| Use the Sum of Product (SOP) Digital Design process to design a Logic Diagram of a logic device using AND, OR and Inverter gates | Able to complete a paper design of a Full Adder (FA) beginning with block diagram progressing to Truth Table, Standard SOP Boolean Equation, minimized SOP Boolean equation via Algebra and also via K-Map, and finally producing a correct logic diagram | **(Formative)** 86% (6 / 7) of students correctly completed all steps of the process. |
| From previous paper design, use Digital Design CAD software to simulate the FA | Students download a free Logisim or DigitalWorks program. Uisng the tool they enter FA logic diagram completed above. Then they test every combination of inputs interactively as well as by timing diagram. | **(Formative)** 100% (7 / 7) of students were able to use DigitalWorks or Logisim to simulate the FA. |
| From the simulated CAD design, implement a FA using Verilog on a DE10 LITE board | Given a DE10 LITE board, students implement the Full Adder (coded in Verilog) with three switches as inputs and two LED’s as outputs. | **(Summative)** 86% (6 / 7) of students, were able to complete the lab building, debugging and demonstrating a Full Adder via DE10 Lite |

**History of Results**: Not Available.

**Faculty Discussion:** (Oct 24 2022) Students met the performance target on this assessment.

**Interpretation**: No improvement needed.

**Assessment B – KF 442**

**Learning Outcome (1):** an ability to apply knowledge, techniques, skills and modern tools of mathematics, science, engineering, and technology to solve broadly defined engineering problems appropriate to the discipline;

**Course/Event:** CST 442 Direct Assessment

**Level**: Capstone

**Assessor & Campus:** Douglas Lynn at Klamath Falls

**Activity**: A question (6d) was given on the CST 442 midterm exam that required students to compute the change in CPI from making jumps – which represent 2% of instructions in a program -- take a different number of cycles (i.e. one cycle as opposed to two). To correctly solve this problem, students have to realize that CPI is a weighted sum and that the contribution to CPI from jumps that take n cycles is n x .02 rather than CPIold x .02. (i.e. CPIold = 1.35 = x + .02 × 2, so CPInew = x + .02 × 1 = 1.35 - .02 × 1 = 1.33) .

**Sample and Reliability**: Ten student artifacts were assessed. Limited sample size may skew results. Scoring was performed by Douglas Lynn.

**Performance Target**: 70% of students correctly formulate the problem or achieve the correct numerical result.

**Assessment Method**:

|  |  |  |
| --- | --- | --- |
| Performance Criteria | Measurement Scale | Results |
| Students properly computed the contribution to CPI from jumps as n x .02 | number that computed the contribution to CPI from jumps as n x .02 | 70% (7/10) of students correctly formulated the problem |

**History of Results**: Students did better on this assessment the last time it was done.

**Faculty Discussion** (Oct 24 2022): Performance just met expectations, doing worse than the last time this assessment was given. Note that this term, the class was taught fully online due to Covid-19 and the exams were also given remotely online which also partly explains the drop in performance

**Interpretation**: No improvement needed.

**Assessment C – KF 418**

**Learning Outcome (1):** an ability to apply knowledge, techniques, skills and modern tools of mathematics, science, engineering, and technology to solve broadly engineering problems appropriate to the discipline;

**Course/Event:** CST 418 Direct Assessment

**Level**: Capstone

**Assessor & Campus:** Douglas Lynn at Klamath Falls

**Activity**: The following question was given in the CST 418 (Networks) final exam:

If the probability of an error in one packet of a message traversing one hop of a network is Ppe, what is the probability that 1 packet can be delivered across an n hop virtual circuit without any errors? To correctly solve this problem, students must realize that Ppne = 1 - Ppe, that n packets have to be transmitted without error and that probabilities from independent events multiply.

**Sample and Reliability**: Six student artifacts were assessed. Limited sample size may skew results. Scoring was performed by Douglas Lynn.

**Performance Target**: 70% of students correctly formulate the problem or achieve the correct numerical result.

**Assessment Method**:

|  |  |  |
| --- | --- | --- |
| Performance Criteria | Measurement Scale | Results |
| Pne = 1 - Pe | correct / incorrect (or not attempted) | 83% (5/6) of students did this correctly |
| Probabilities multiply | correct / incorrect (or not attempted) | 83% (5/6) of students did this correctly |

**History of Results**: Students did better on this assessment than the last time it was given.

**Faculty Discussion** (Oct 24 2022): Performance exceeded expectations.

**Interpretation**: No improvement needed.

**Assessment D – Exit Survey**

**Learning Outcome (1):** an ability to apply knowledge, techniques, skills and modern tools of mathematics, science, engineering, and technology to solve broadly defined engineering problems appropriate to the discipline;

**Course/Event:** 2020-21 Senior Exit Survey Indirect Assessment

**Level**: Capstone

**Assessor & Campus:** Barb Meng at Klamath Falls

**Activity**: Questions related to this outcome asked on the Senior Exit survey were:  
Q BCMP 1 - Program Student Learning Outcomes for Computer Engineering Technology B.S. Please rate your proficiency in the following areas.

a. An ability to select and apply the knowledge, techniques, skills, and modern tools of the discipline to broadly-defined engineering technology activities.  
b. An ability to select and apply a knowledge of mathematics, science, engineering, and technology to engineering technology problems that require the application of principles and applied procedures or methodologies.  
d. An ability to design systems, components, or processes for broadly-defined engineering technology problems appropriate to program educational objectives.

**Sample and Reliability**: Only one BCMP student responded to this question on the Senior exit survey, so the results aren’t statistically reliable.

**Performance Target**: 70% of students rate their performance as Highly proficient or Proficient

**Assessment Method**:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Performance Criteria | High Proficiency | Proficiency | Some Proficiency | Low Proficiency |
| Q BCMP 1a | (0/1) 0% | (1/1) 100% | (0/1) 0% | (0/1) 0% |
| Q BCMP 1b | (0/1) 0% | (1/1) 100% | (0/1) 0% | (0/1) 0% |
| Q BCMP 1d | (1/1) 100% | (0/1) 0% | (0/1) 0% | (0/1) 0% |

**History of Results**: Data from surveys completed in previous years also show that students consistently rate themselves as Highly Proficient or Proficient on this outcome.

**Faculty Discussion** (Oct 24 2022): Performance exceeded expectations.

**Interpretation**: No improvement needed.

**Assessment E – KF/Wil 337**

**Learning Outcome (4):** an ability to conduct standard tests, measurements, and experiments and to analyze and interpret the results;

**Course/Event:** CST 337 Direct Assessment

**Level**: Capstone

**Assessor & Campus:** Douglas Lynn at Klamath Falls and Wilsonville (remote delivery)

**Activity**: Students in CST 337 were required to use a logic analyzer to identify and measure (among other parameters) MOSI setup (T5) and hold (T6) provided to an SPI based EEProm chip by a PIC32 processor and the MISO setup (SP40) and hold (SP41) provided to a PIC32 processor by the EEProm chip.

**Sample and Reliability**: Eight student artifacts were assessed. Limited sample size may skew results. Scoring was performed by Douglas Lynn.

**Performance Target**: 100% of students need to be able to setup and use the Logic analyzer with minimal assistance. 70% of students need to be able to correctly identify and measure the setup and hold times.

**Assessment Method**:

|  |  |  |
| --- | --- | --- |
| Performance Criteria | Measurement Scale | Results |
| Student was able to properly setup the logic analyzer | Able / needed assistance | 100% (8/8) |
| T5 correctly measured. | correct / incorrect (or not attempted) | 87.5% (7/8) |
| SP40 correctly measured. | correct / incorrect (or not attempted) | 87.5% (7/8) |
| T6 correctly measured. | correct / incorrect (or not attempted) | 87.5% (7/8) |
| SP41 correctly measured. | correct / incorrect (or not attempted) | 87.5% (7/8) |

**History of Results**: Not available

**Faculty Discussion** (Oct 24, 2022): All but one student demonstrated the ability to identify setup and hold. Students occasionally confuse the MISO setup and hold with the MOSI setup and hold, or just don’t label their screenshots, but this is more of a documentation issue.

**Interpretation**: No improvement needed. Next time the assignment is given, more emphasis will be given on labelling their screenshots.

**Assessment F – KF 315**

**Learning Outcome (4):** an ability to conduct standard tests, measurements, and experiments and to analyze and interpret the results;

**Course/Event:** CST 315 Direct Assessment

**Level**: Capstone

**Assessor & Campus:** George Drouant at Klamath Falls

**Activity**: Lab 8 is the culmination of a four lab sequence. In Lab 8 the students construct a feedback control system that uses a microcontroller to control the water level in a small bucket. The water level is sensed by a capacitive sensor that the students built in Lab 1. In Lab 3 the sensor is used as part of a relaxation oscillator whose output frequency changes with the sensor’s capacitance – the sensor’s capacitance changes with the level of water in a bucket. The students then learned how to interface a microcontroller to a high current load using a n-channel enhancement MOSFET in Lab 7. Lab 8 ties these activities together to produce a water level control system that senses the water level in a bucket and uses a microcomputer to control a pump motor to set the water level to a desired height. A rubric was used to assess student performance

**Rubric**:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | High Proficiency | Proficiency | Some Proficiency | Limited or no Proficiency |
| Understanding of Technical Problem | Clearly defines the problem and outlines necessary objectives in an efficient manner. | Problem statement has some ambiguity or misses some important issues | Problem is defined incorrectly or too narrowly. Key information is missing or incorrect | Problem not defined at all |
| Design of system to solve problem | can describe planned experiments and how they relate to the problem; relate hypotheses to previous knowledge; | Description of planned experiments, relation of hypotheses, identification of steps and timeline, can be accomplished | Fails to formulate hypotheses to test.  Does not express possible outcomes. | No clue on how to solve problem |
| Tools | Consistently uses new procedures and tools successfully, and can describe rationale for them. Runs appropriate control and replicate experiments | Uses new methods and tools, but may not always be successful. May not accurately explain rationale. Control and replicate experiments run | Errors made in analytical methods, but sources of error aren’t found. Appropriate control or replicate experiments not run. | Unfamiliar with rudimentary electrical measurement tools |

**Sample and Reliability**: 24 student artifacts were assessed. Scoring was performed by George Drouant.

**Performance Target**: 70% of students need to be able to demonstrate performance at the Proficiency or High Proficency levels.

**Assessment Method**:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Performance Criteria | High Proficiency | Proficiency | Some Proficiency | No/Limited Proficiency |
| Understanding of the technical problem | 19 | 5 |  |  |
| Design solution to problem | 19 | 5 |  |  |
| Tools | 19 | 5 |  |  |

**History of Results**: Not available.

**Faculty Discussion** (Oct 24, 2022): In this assessment 100% of students met the performance criteria.

**Interpretation**: No changes need to be made as a result of this assessment.

**Assessment G – Wil - 473**

**Learning Outcome (4):** an ability to conduct standard tests, measurements, and experiments and to analyze and interpret the results;

**Course/Event:** CST 473 Direct Assessment

**Level**: Capstone

**Assessor & Campus:** Phong Nguyen at Wilsonville

**Activity**: Students enrolled in Senior Project were asked to cpmplete a “Lessons Learned” paper in which they were asked to provide examples of failures in their senior projects, to write about experiments, tests, analysis of failures and to write about how to improve their processes so as to minimize the likelihood of making the same failure in the future.

**Sample and Reliability**: 5 student papers were assessed. Limited sample size may skew results. Scoring was performed by Phong Nguyen.

**Performance Target**: 70% of students need to be able to score 80% or higher on the paper.

**Assessment Method**:

|  |  |  |
| --- | --- | --- |
| Performance Criteria | Measurement Scale | Results |
| Student score on paper | 80% or better | 59% (5/9) of students scored 80% or better |

**History of Results**: An assessment related to this one was previously done in Spring 2018 and 100% of the 6 students in the class met the performance criteria on that assessment.

**Faculty Discussion** (Oct 24 2022): Of the students that did complete the course, 100% (5/5) received a score of 80% or better on this paper demonstrating proficiency for the purposes of this assessment. \*Four of the nine students originally enrolled in the class took an Incomplete in the class and did not complete this paper. Covid had much to do with this as it brought all manners of issues which resulted in incompletes.

**Interpretation**: No changes need to be made as a result of this assessment.

**Assessment H – Exit Survey**

**Learning Outcome (4):** an ability to conduct standard tests, measurements, and experiments and to analyze and interpret the results;

**Course/Event:** 2020-21 Senior Exit Survey Indirect Assessment

**Level**: Capstone

**Assessor & Campus:** Barb Meng at Klamath Falls

**Activity**: Questions related to this outcome asked on the Senior Exit survey were:  
Q BCMP 1 - Program Student Learning Outcomes for Computer Engineering Technology B.S. Please rate your proficiency in the following areas.

c. An ability to conduct standard tests and measurements; to conduct, analyze, and interpret experiments; and to apply experimental results to improve processes.

**Sample and Reliability**: Only one BCMP student responded to this question on the Senior exit survey, so the results aren’t statistically reliable.

**Performance Target**: 70% of students rate their performance as Highly proficient or Proficient

**Assessment Method**:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Performance Criteria | High Proficiency | Proficiency | Some Proficiency | Low Proficiency |
| Q BCMP 1c | (0/1) 0% | (1/1) 100% | (0/1) 0% | (0/1) 0% |

**History of Results**: Data from surveys completed in previous years also show that students consistently rate themselves as Highly Proficient or Proficient on this outcome.

**Faculty Discussion** (Oct 24, 2022): Performance exceeded expectations.

**5**

**Interpretation**: No improvement needed.

**Program Improvement Discussions** (Sep 18, 2020)

The mission statement for Computer Engineering Technology was reviewed.

No changes were made.

The mission statement for Embedded Systems Engineering Technology was reviewed.

No changes were made.

The Program Educational Objectives for Computer Engineering Technology were reviewed.

No changes were made.

The Program Educational Objectives for Embedded Systems Engineering Technology were reviewed

No changes were made.

**Appendix A**

**OREGON INSTITUTE OF TECHNOLOGY**

**Computer Systems Engineering Technology Department**

***CST 315 – Embedded Sensor Interfacing I/O***

**Lab 8 – Water Level Control System**

**EQUIPMENT AND SUPPLIES:**

* Oscilloscope with probes
* Set of probes for DMM
* Alligator clip cables to connect to the bench power supply
* 330 Ohm resistor
* 220 Ohm resistor
* 1 Meg resistor
* 3 – 100K resistors
* 2 – 3.3K resistors
* 2 – 10K resistors
* Water level sensor
* LM393 Comparator
* 4N33 Optoisolator
* TN0610N3-G N-Channel MOSFET
* Arduino microcontroller
* Pump motor with tubing
* Diode (1N4004)
* 2 – plastic buckets

In today’s lab you will construct a microcontroller based water level control system – see diagrams below. You will use the water level sensor you built and tested, along with the relaxation oscillator you constructed from the LM393 comparator. The second half of the LM393 will be used as a buffer between the water level sensor and the input of the Arduino microcontroller (Arduino pin 8 is suggested as the input pin). The Arduino will control the operation of a pump motor – you may use a simple on/off control scheme or one based on pulse width modulation to control the pump. The pump motor control circuit is the same circuit you constructed to operate a relay in the last lab with the exceptions that the relay is replaced by the pump, and the voltage is reduced from 12V to 5V.

Your system will pump water from Bucket A (initially filled with water) to Bucket B (initially empty). The control system will fill Bucket B to a depth of three inches. When a depth of three inches is reached the system will stop filling Bucket B. The pump must not turn on again unless water is removed from Bucket B. The instructor will use a cup to transfer water from Bucket B to Bucket A. The control system will detect the drop in water level and again fill Bucket B to three inches of water.



**Figure 1**



Figure 2



Figure 3